UM74HCT612

Memory Mapper

Features

- Fully compatible with TTL, NMOS and CMOS devices.
- Expands 4 address lines to 12 address lines.
- Designed for paged memory mapping.
- High-current 3-state outputs.

General Description

The UM74HCT612 essentially contains a 4-line to 16-line decoder and a 16-word by 12-bit RAM. It is designed to expand a microprocessor's memory address capability by 8 bits (from 4 to 12). That is, four bits of the memory address bus can be used to select one of 16 map registers that contain 12 bits each. These 12 bits are presented to the system memory address bus along with the unused memory address bit from the CPU. By periodically re-loading the mapper registers from the data bus, one can access any of the 16 pages of memory.

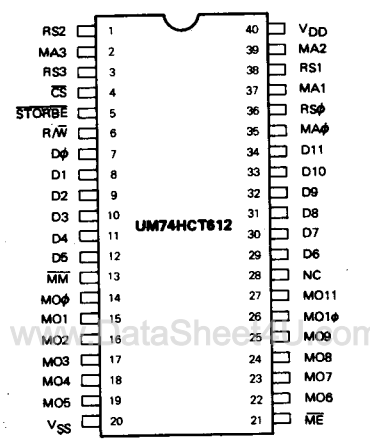
There are four modes of operation (read, write, map, and pass). When $\overline{CS}$ (Chip Select) is active low, through $D_0 \sim D_7$, data may be read from or written into the map register selected by the register select inputs (RSϕ ~ RS3) under the control of R/$\overline{W}$.

When $\overline{CS}$ is high and $\overline{MM}$ (Map Mode Control) is active low, the map operation will output the contents of map register selected by the map address input (MAϕ ~ MA3).

When $\overline{CS}$ and $\overline{MM}$ are both high (pass mode), the address bit on MAϕ ~ MA3 appears at MO8 ~ MO11, respectively, with the other bits forcing low level. MO0 ~ MO7 are low.

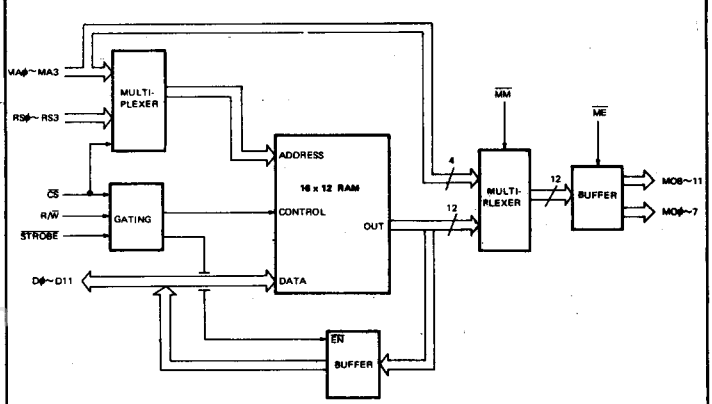
All outputs are tri-state outputs with high current capability. The $\overline{STROBE}$ input is used to enter data into selected map register during I/O operation. Map outputs are enabled by the $\overline{ME}$ input.

Pin Configuration



*NC: Not connected.

Block Diagram



Absolute Maximum Ratings*

D.C. Supply Voltage, V_{DD} ..... −0.5V to 7V (respect to V_{SS})

Operating Temperature ..... 0°C to 70°C

Storage Temperature ..... −65°C to 150°C

Comments*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(T_A = 25°C, V_{DD} = 5V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Power Supply	4.5	5	5.5	V	Recommended
V_{IH}	Input High-Level Voltage	2.0	–	–	V	Recommended
V_{IL}	Input Low-Level Voltage	–	–	0.8	V	Recommended
V_{OHD}	Output High-Level Voltage on D0 ~ D11	4.4	4.9	–	V	I_{OH} = −20 μA
		3.8	4.0	–	V	I_{OH} = −6.0 mA
V_{OHM}	Output High-Level Voltage on MOϕ ~ MO11	4.4	4.9	–	V	I_{OH} = −20 μA
		3.8	4.3	–	V	I_{OH} = −8.0 mA
V_{OLD}	Output Low-Level Voltage on D0 ~ D11	–	0.001	0.1	V	I_{OL} = 20 μA
		–	0.3	0.4	V	I_{OL} = 12 mA
V_{OLM}	Output Low-Level Voltage on MOϕ ~ MO11	–	0.001	0.1	V	I_{OL} = 20 μA
		–	0.4	0.5	V	I_{OL} = 20 mA
I_{IN}	Input Current	−1.0	–	1.0	μA	V_{IN} = 5V ~ 0V
I_{OZ}	OFF-State Output Current	−5	–	5	μA	V_o = 3V ~ 0V
I_{CC}	Steady Current Consumption	–	–	10	μA	V_{IN} = V_{DD} or 0V, No Load.

Timing Requirement and Switching Characteristics:

Parameter	Min.	Typ.	Max.	Unit	Condition
Pulse Width of $\overline{STROBE}$: Tsbw	75	–	–	ns	Recommended Value
$\overline{CS}$ Setup Time: Tcssu ($\overline{CS}$ low to $\overline{STROBE}$ low)	20	–	–	ns	Recommended Value
R/$\overline{W}$ Setup Time: Trwsu (R/W low to $\overline{STROBE}$ low)	20	–	–	ns	Recommended Value
RS Setup Time: Trssu (RS valid to $\overline{STROBE}$ low)	20	–	–	ns	Recommended Value
DATA Setup Time: Tdasu (D0–D11 valid to $\overline{STROBE}$ high)	75	–	–	ns	Recommended Value
CS Hold Time: Tcshd ($\overline{STROBE}$ high to $\overline{CS}$ high)	20	–	–	ns	Recommended Value
R/$\overline{W}$ Hold Time: Trwnd ($\overline{STROBE}$ high to R/$\overline{W}$ high)	20	–	–	ns	Recommended Value
RS Hold Time: Trshd ($\overline{STROBE}$ high to RS invalid)	20	–	–	ns	Recommended Value
DATA Hold Time: Tdahd ($\overline{STROBE}$ high to D0–D11 invalid)	20	–	–	ns	Recommended Value
RS to D0–D11: TRSDV (TpHL or TpLH)	–	39	75	ns	Figure 1 with RL = 1K, CL = 50P. Timing Diagram see Figure 6.
$\overline{CS}$ ↓ to D0–D11: TCLDV (TpZL or TpZH)	–	26	50	ns	
$\overline{CS}$ ↑ to D0–D11, disable: TCHDZ (TpHZ or TpLZ)	–	38	65	ns	
R/$\overline{W}$ ↑ to D0–D11: TWHDV (TpZL or TpZH)	–	20	35	ns	
R/$\overline{W}$ ↓ to D0–D11, disable: TWLDZ (TpHZ or TpLZ)	–	30	50	ns	
$\overline{CS}$ ↑ to MOϕ–MO11: TCHQ (TpHL or TpLH)	–	48	85	ns	Figure 1 with RL = 1K; CL = 50P. Timing Diagram see Figure 7.
$\overline{MM}$ ↓ to MOϕ–MO11: TMLQ (TpHL or TpLH)	–	20	40	ns	
$\overline{MM}$ ↑ to MOϕ–MO11: TMHQ (TpHL or TpLH)	–	22	40	ns	
MA to MOϕ–MO11, $\overline{MM}$ = low: TAVQ1 (TpHL or TpLH)	–	39	70	ns	
MA to MO8–MO11, $\overline{MM}$ = high: TAVQ2 (TpHL or TpLH)	–	13	30	ns	
$\overline{ME}$ ↓ to MOϕ–MO11: TELQ (TpZL or TpZH)	–	17	30	ns	
$\overline{ME}$ ↑ to MOϕ–ME11, disable: TEHQZ (TpHZ or TpLZ)	–	14	25	ns	

Note: See Figures 2, 3, 4, and 5, for definitions of TpLH, TpHL, TpHZ, TpLZ, TpZH, TpZL.

Pin Description

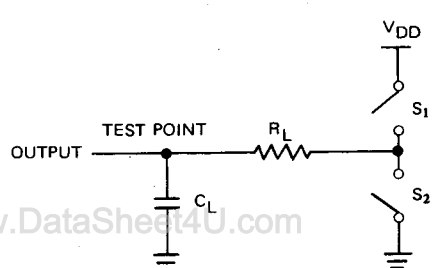
Pin Name	Function Description
Dϕ–D11	I/O connection to data and control bus is used for reading from or writing into the map register.
RSϕ–RS3	Register select inputs for I/O operation.
R/$\overline{W}$	Read or write control pin is used in I/O operation. When low, data bus is used to write into register. When high, data bus is used to read from register.
$\overline{STROB}$	Strobe input is used to enter data into register.
$\overline{CS}$	Chip select input. When low, the Read and Write Modes are active.
MAϕ–MA3	Inputs to select one of 16 registers, when in map mode.
MOϕ–MO11	Map outputs. Present the map register contents to the system memory address bus in the map mode. When in pass mode, these outputs provide the map address data on MO8 – MO11 and low level on MOϕ–MO11.
$\overline{MM}$	Map mode input. When low, the map mode is active; when high, it is pass mode.
$\overline{ME}$	Map output enable pin. When low, outputs MOϕ–MO11 are active. When high, these is high impedance.

Function Table

$\overline{CS}$	$\overline{MM}$	R/$\overline{W}$	$\overline{STROBE}$	Operation
0	X	0	0	Write Mode, D0 ~ D7 ⇒ Selected Register.
0	X	1	X	Read Mode, Selected Register ⇒ Dϕ ~ D7.
1	0	X	X	Map Mode, Register Contents ⇒ MOϕ ~ MO11 (If $\overline{ME}$ = 0).
1	1	X	X	Pass Mode. MAϕ ~ MA3 ⇒ MD8 ~ MD11 and MDϕ ~ MD7 are all low (If $\overline{ME}$ = 0).

Parameter Measurement

3-State Output



Parameter	S_1	S_2
TpHL	Open	Open
TpLH		
TpZH	Open	Closed
TpHZ		
TpZL	Closed	Open
TpLE		

Figure 1

Set-Up and Rise, Fall Times

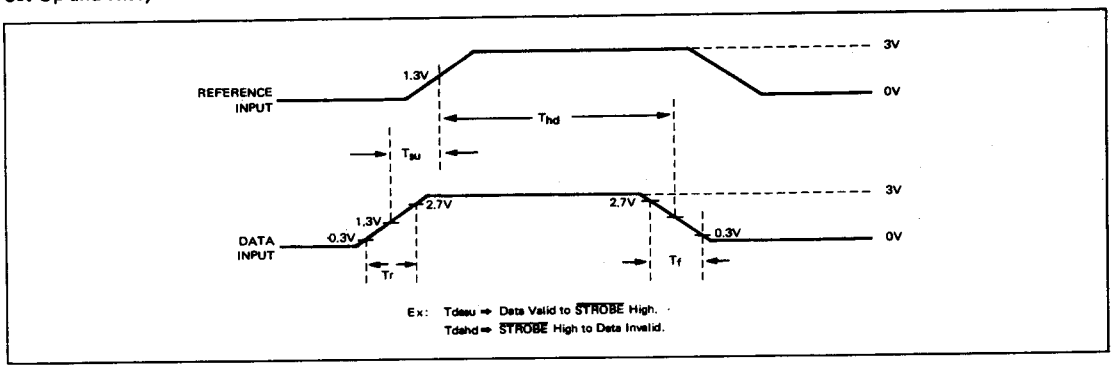


Figure 2

Pulse Duration

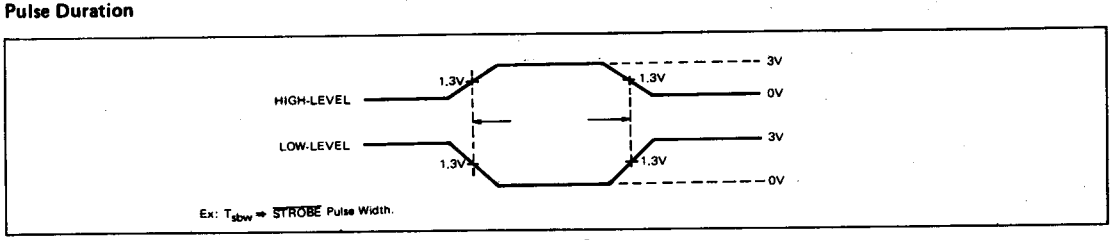


Figure 3

Delay Times

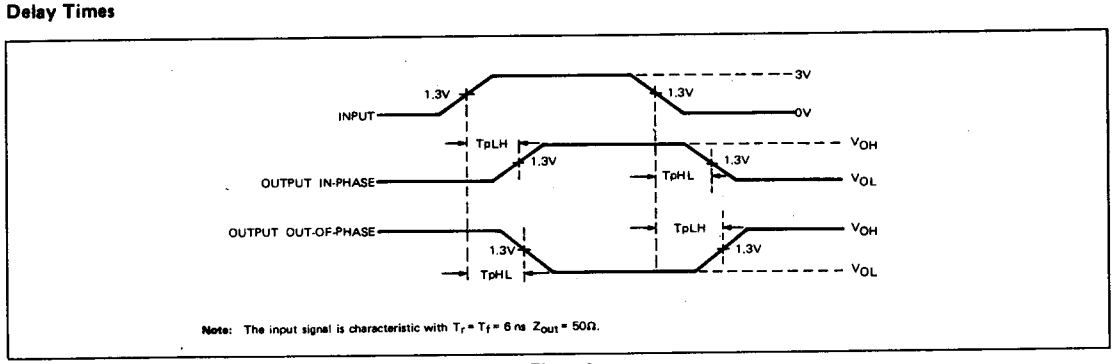


Figure 4

Enable or Disable

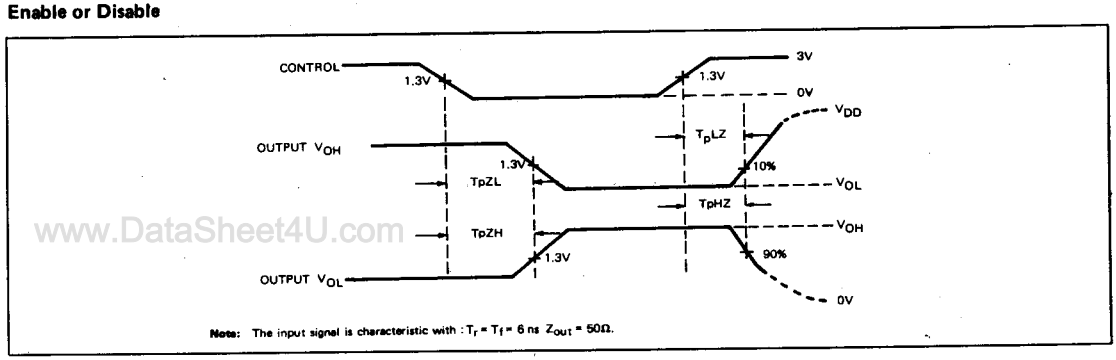


Figure 5

Timing Diagram:

Read and Write Mode

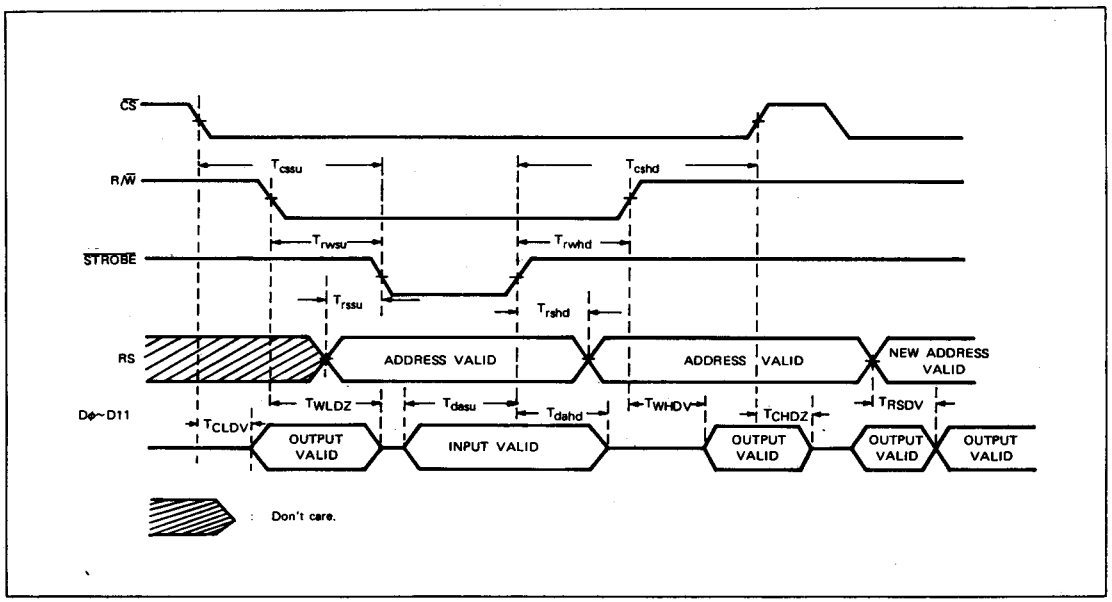


Figure 6

Map and Pass Mode

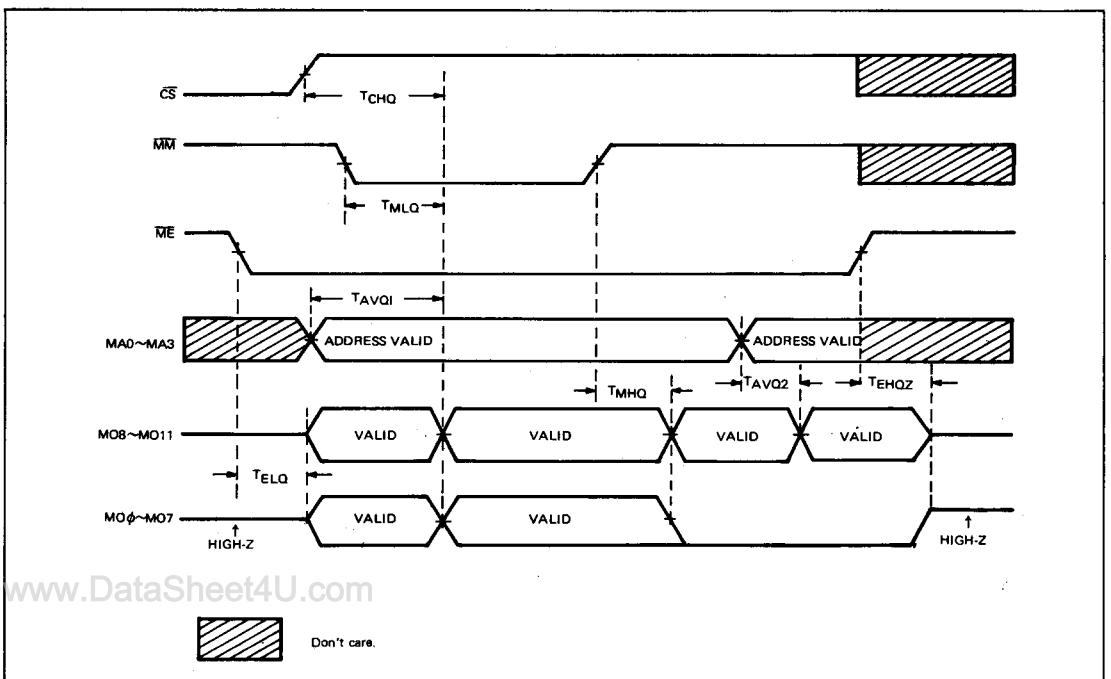


Figure 7