- **Operates From Single 5-V Power Supply**
- **Wide Common-Mode Voltage Range**
- **High Input Impedance**
- **TTL-Compatible Outputs**
- **High-Speed Schottky Circuitry**
- **8-Pin Dual-In-Line Packages**
- **Designed to Be Interchangeable With National DS9639AC**

P PACKAGE
(TOP VIEW)

|			
V_{CC}	1	8	1IN+
1OUT	2	7	1IN−
2OUT	3	6	2IN+
GND	4	5	2IN−
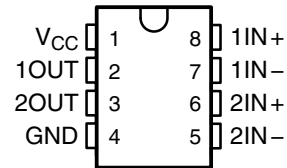
description

The uA9639C is a dual differential line receiver designed to meet ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B and ITU Recommendations V.10 and V.11. It utilizes Schottky circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. This device operates from a single 5-V power supply and is supplied in an 8-pin, dual-in-line package.

The uA9639C is characterized for operation from 0°C to 70°C.

logic symbol†

1IN+	8	
1IN−	7	→ 2 1OUT
2IN+	6	
2IN−	5	→ 3 2OUT
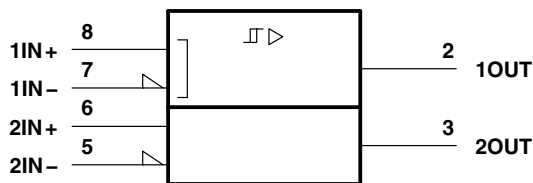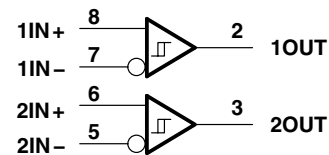
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram

1IN+	8	
1IN−	7	→ 2 1OUT
2IN+	6	
2IN−	5	→ 3 2OUT

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

TYPICAL OF ALL OUTPUTS
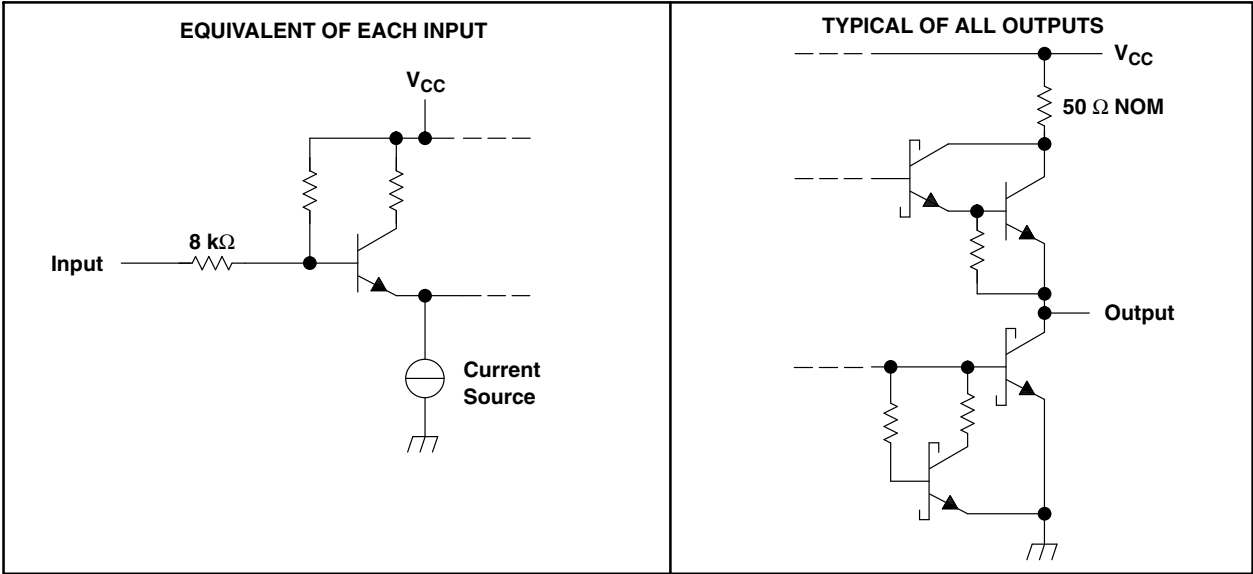
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) .... −0.5 V to 7 V
Input voltage, V_I .... ±15 V
Differential input voltage, V_{ID} (see Note 2) .... ±15 V
Output voltage range, V_O (see Note 1) .... −0.5 V to 5.5 V
Low-level output current, I_{OL} .... 50 mA
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	See Note 3				0.2	V
						0.4	
V_{IT-}	Negative-going input threshold voltage	See Note 3		−0.2			V
				−0.4[‡]			
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				70		mV
V_{OH}	High-level output voltage	$V_{ID} = 0.2$ V,	$I_O = -1$ mA	2.5	3.5		V
V_{OL}	Low-level output voltage	$V_{ID} = -0.2$ V,	$I_O = 20$ mA		0.35	0.5	V
I_I	Input current	$V_{CC} = 0$ to 5.5 V, See Note 4	$V_I = 10$ V		1.1	3.25	mA
			$V_I = -10$ V		−1.6	−3.25	
I_{OS}	Short-circuit output current[§]	$V_O = 0$,	$V_{ID} = 0.2$ V	−40	−75	−100	mA
I_{CC}	Supply current	$V_{ID} = -0.5$ V,	No load		35	50	mA

[†] All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.

[‡] The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

[§] Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

NOTES: 3. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
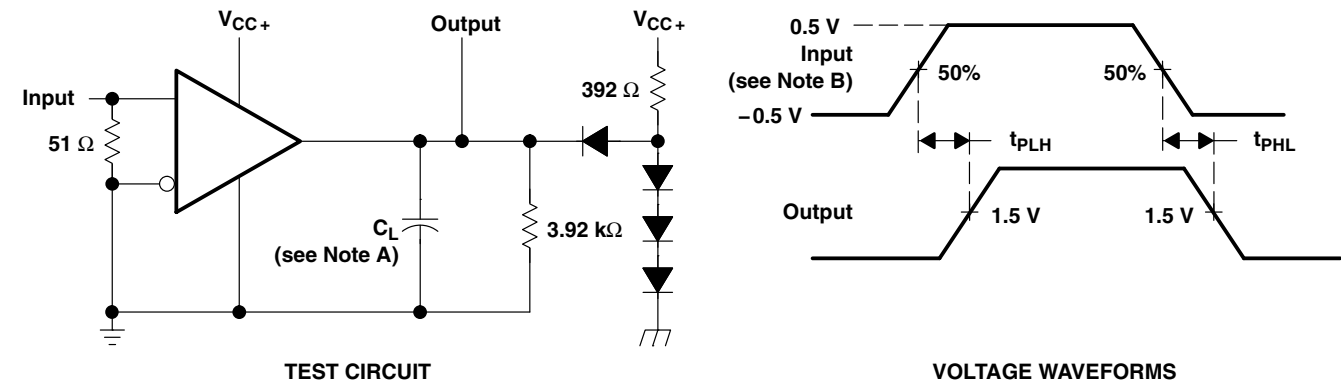4. The input not under test is grounded.

switching characteristics, $V_{CC} = 5$ V, $T_A = 0$°C to 70°C

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$C_L = 50$ pF, See Figure 1		85	ns
t_{PHL}	Propagation delay time, high- to low-level output			85	ns

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
          B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 5 MHz, duty cycle = 50%.

Figure 1. Test Circuit and Voltage Waveforms
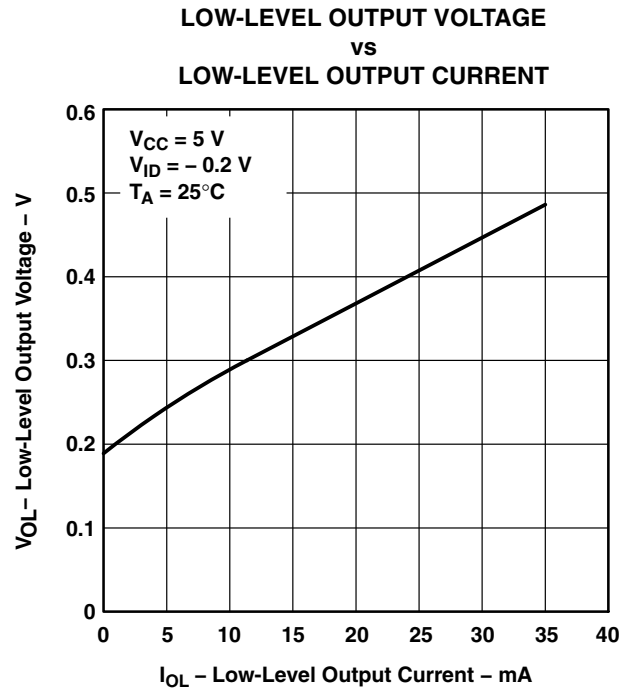
TYPICAL CHARACTERISTICS
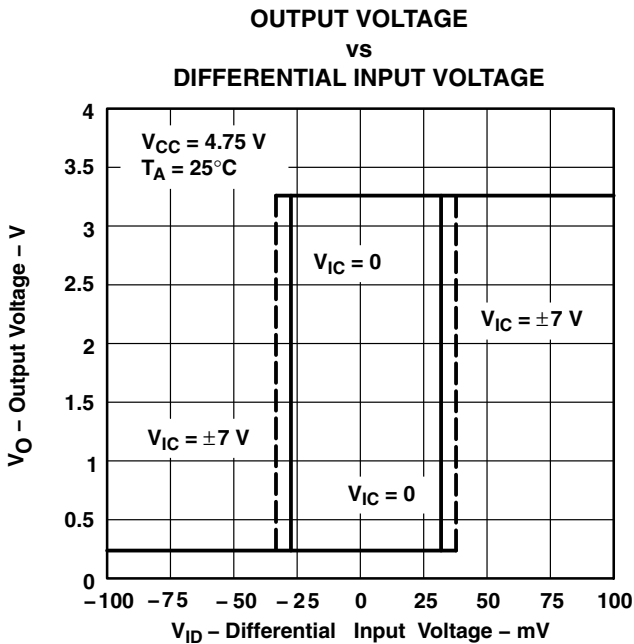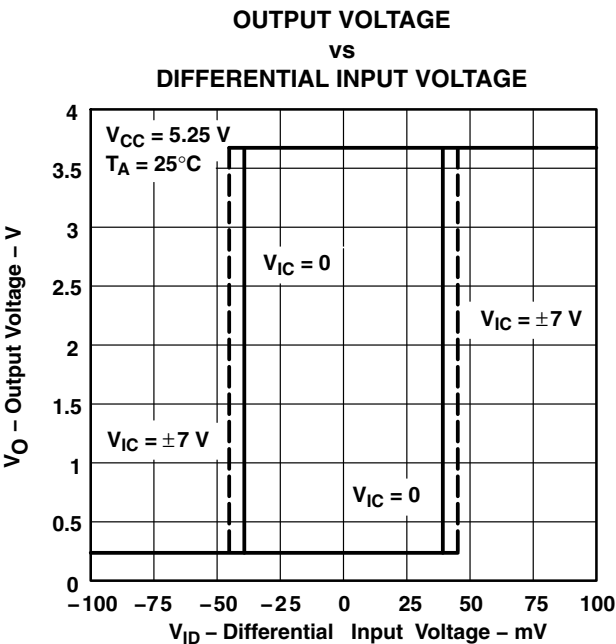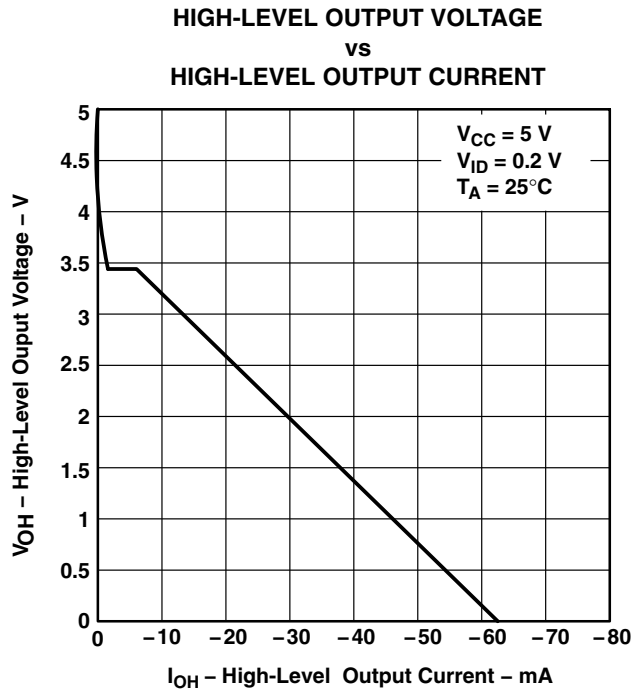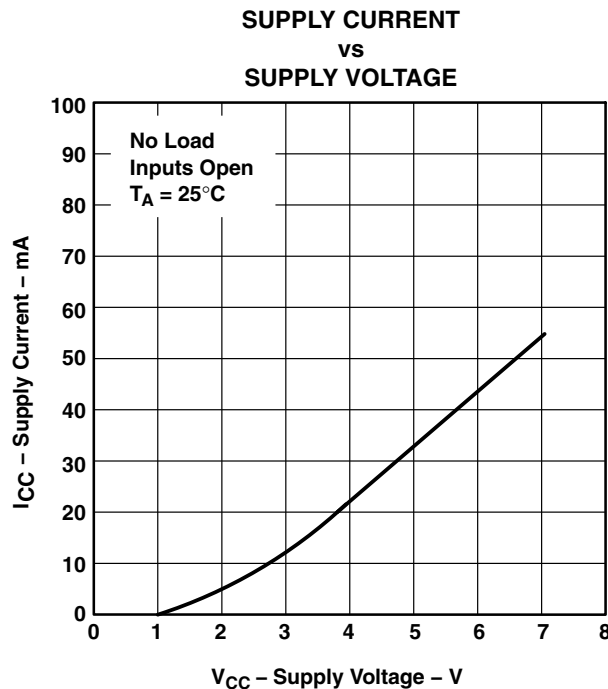
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 2

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 3

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TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

$V_{CC} = 5$ V
$V_{ID} = 0.2$ V
$T_A = 25°C$

V_{OH} – High-Level Ouput Voltage – V

I_{OH} – High-Level Output Current – mA

Figure 4

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

$V_{CC} = 5$ V
$V_{ID} = -0.2$ V
$T_A = 25°C$

V_{OL} – Low-Level Output Voltage – V

I_{OL} – Low-Level Output Current – mA

Figure 5

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

**No Load
Inputs Open
$T_A = 25°C$**

I_{CC} – Supply Current – mA

V_{CC} – Supply Voltage – V

Figure 6

TEXAS
INSTRUMENTS

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5

APPLICATION INFORMATION
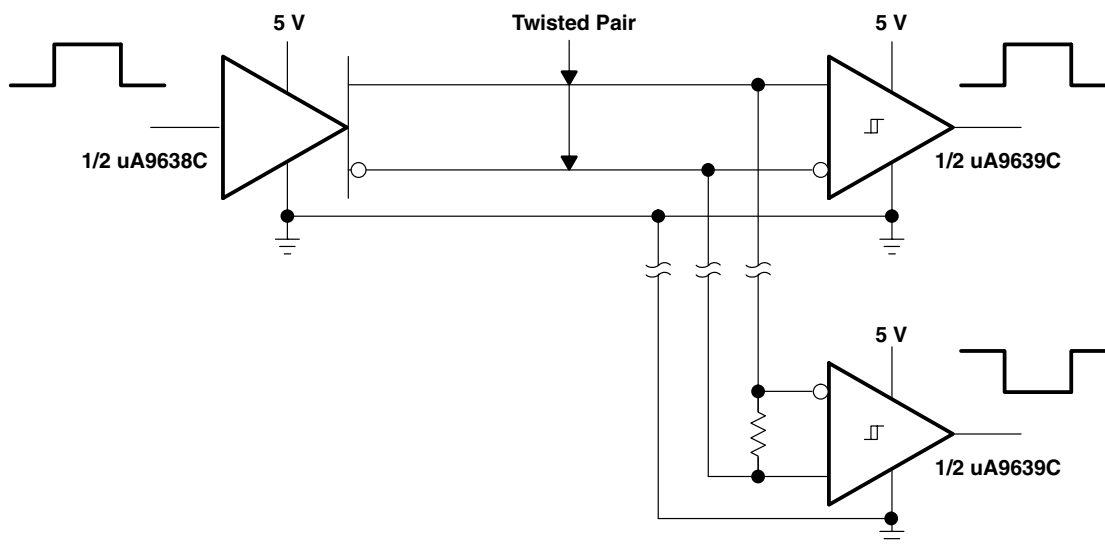
Figure 7. EIA/TIA-422-B System Applications

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
UA9639CD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
UA9639CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
UA9639CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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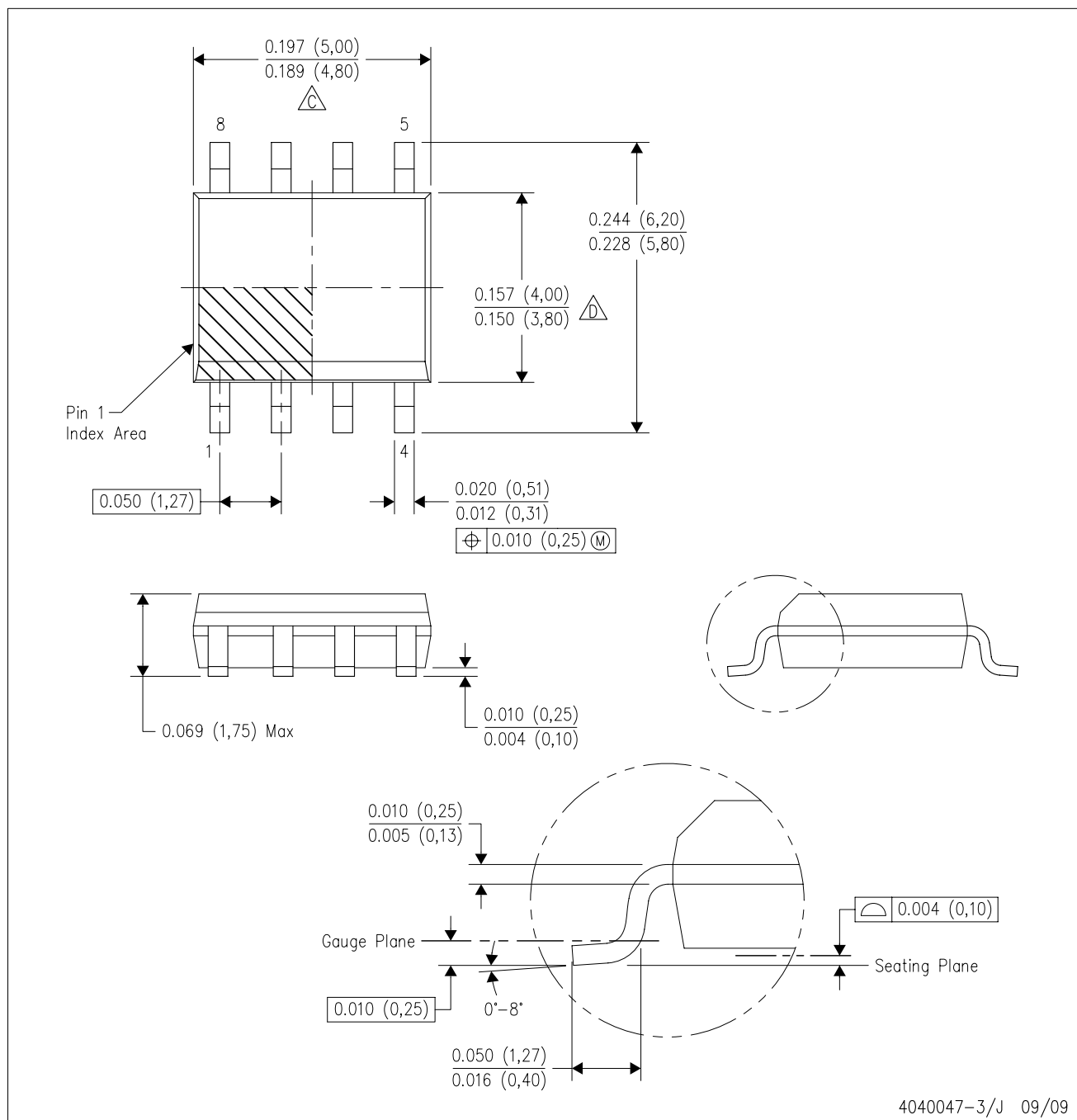P (R−PDIP−T8)   PLASTIC DUAL−IN−LINE PACKAGE
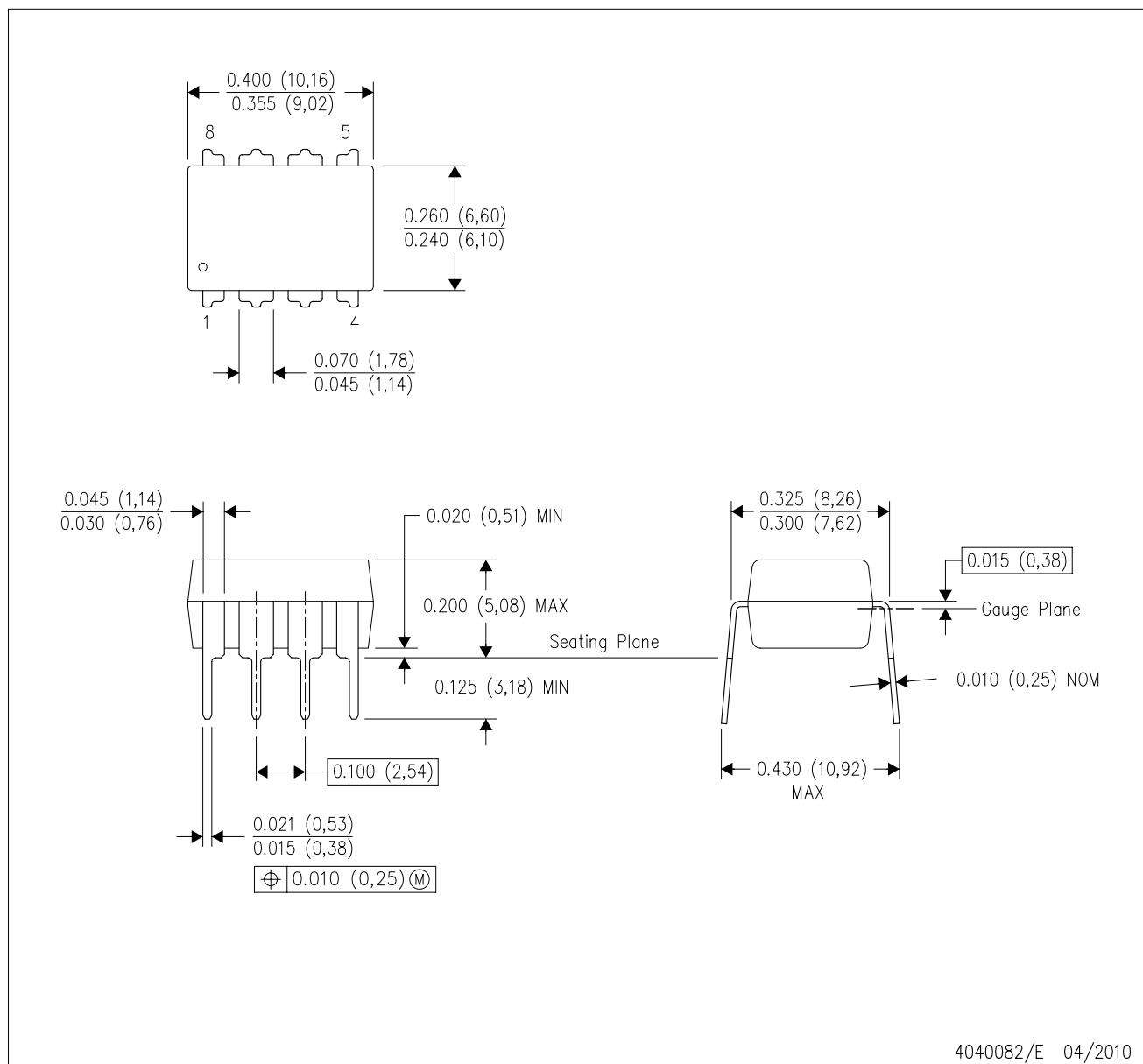
0.400 (10,16) / 0.355 (9,02)

8   5

0.260 (6,60) / 0.240 (6,10)

1   4

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040082/E   04/2010

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MS−001 variation BA.

D (R−PDSO−G8) PLASTIC SMALL−OUTLINE PACKAGE

0.197 (5,00)
0.189 (4,80)
C

8   5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) D

Pin 1
Index Area

1   4

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) M

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

0.004 (0,10)

Seating Plane

4040047−3/J 09/09

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
        D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
        E. Reference JEDEC MS−012 variation AA.

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