TOSHIBA MOS MEMORY PRODUCT

65,536 WORD × 8 BIT N-MOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
PRELIMINARY

TMM27512D-20,TMM27512D-200
TMM27512D-25,TMM27512D-250

DESCRIPTION

The TMM27512D is a 65,536 word × 8 bit ultraviolet light erasable and electrically programmable read memory.

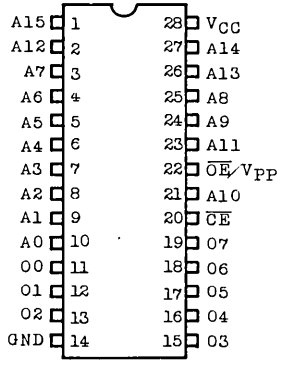
For read operation, the TMM27512D's access time is 200ns/250ns. The TMM27512D operates from a single 5-volt power supply and has a low power standby mode which reduces power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. For program operation, the programming is achieved by using the high speed prgramming mode. The TMM27512D is fabricated with N-channel silicon double layer gate MOS technology.

FEATURES

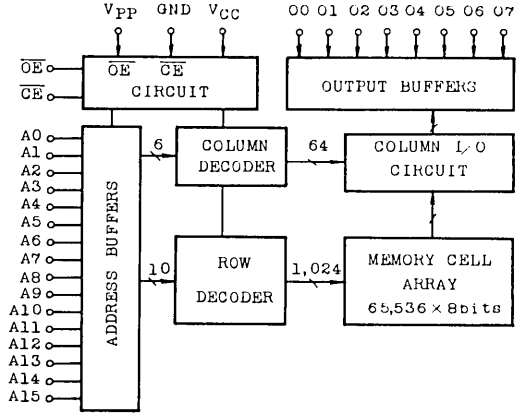
	−20	−25	−200	−250
V_{CC}	5V±5%		5V±10%	
t_{ACC}	200ns	250ns	200ns	250ns
I_{CC2}	120mA		130mA	
I_{CC1}	35mA		40mA	

- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with i27512
- Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{15}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}/V_{PP}$	Output Enable Input / Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read	L	L	5V	Data Out	Active
Output Deselect	*	H		High Impedance	
Standby	H	*		High Impedance	Standby
Program	L	V_{PP}	6V	Data In	Active
Program Inhibit	H	V_{PP}		High Impedance	
Program Verify	L	L		Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_{STG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	0~70	°C

READ OPERATION

D. C. AND RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27512D-20/25	TMM27512D-200/250
Ta	Operating Tamperature	0~70°C	0~70°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%

D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}		—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}		—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	−20/25	—	—	35	mA
			−200/250	—	—	40	
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	−20/25	—	—	120	mA
			−20/250	—	—	130	
V_{IH}	Input High Voltage	—		2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	—		−0.3	—	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA		2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6		—	—	±10	μA

A. C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM27512D-20/200		TMM27512D-25/250		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	200	—	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	200	—	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	90	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns

A. C. TEST CONDITIONS

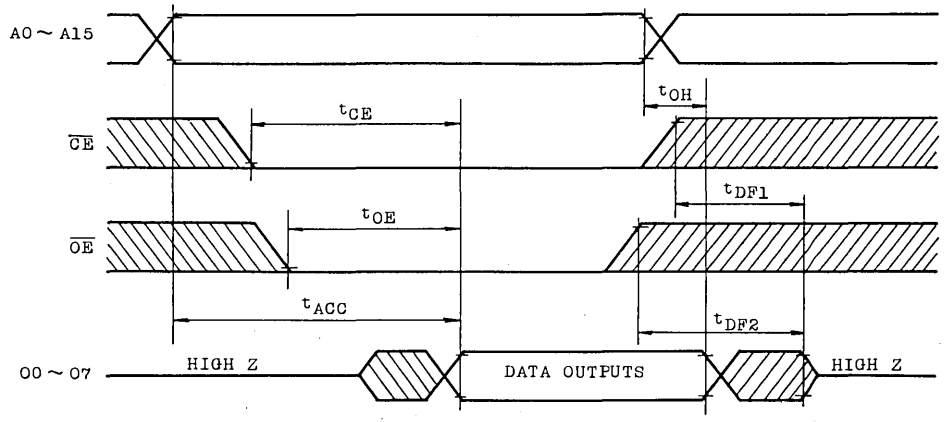
- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance	$V_{IN}=0V$	—	4	6	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN}=0V$	—	50	60	pF
C_{OUT}	Output Capacitance	$V_{OUT}=0V$	—	8	12	pF

* This paramater is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Outpu Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	130	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA
V_{ID}	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

A. C. PROGRAMMING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	—	2	—	—	μs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	—	2	—	—	μs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time	—	50	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time	—	2	—	—	μs
t_{VCS}	V_{CC} Setup Time	—	2	—	—	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}/V_{PP}=V_{PP}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE}/V_{PP}=V_{IL}$	—	—	1	μs
t_{DF}	$\overline{CE}$ to Output in High-Z	$\overline{OE}/V_{PP}=V_{IL}$	—	—	130	ns

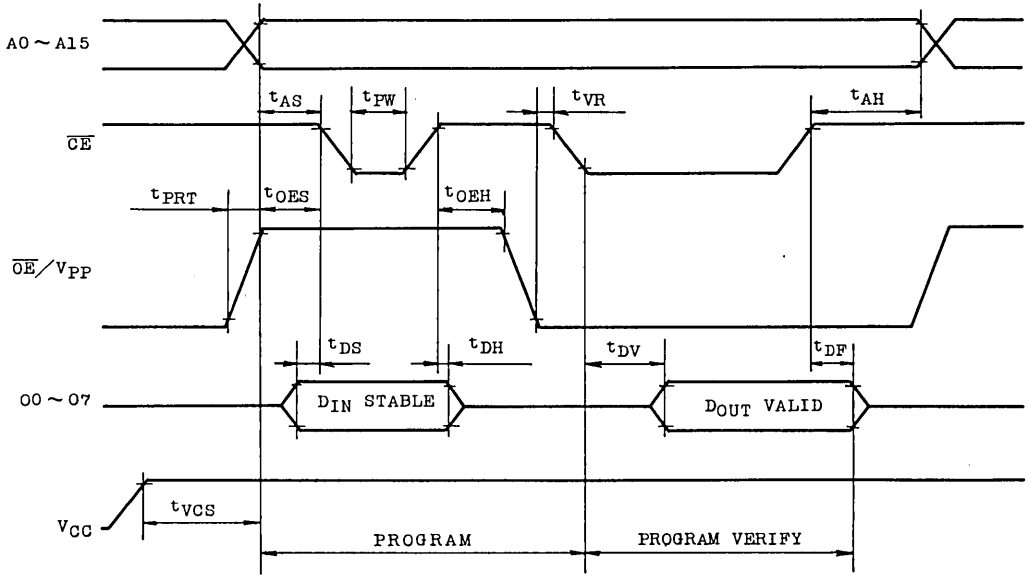
A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note: (1) V_{CC} must be applied simultaneously with or before V_{PP} and cut off simultaneously with or after V_{PP}.
(2) Removing the device from the socket and setting the device in the socket with V_{PP}=12.5V may cause permanent damage to the device.
(3) The V_{PP} supply voltage is permitted up to 14V for program operation; Voltages over 14V should be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not exceed 14V.

ERASURE CHARACTERISTICS

The TMM27512D's erasure is achieved by applying shortwave ultraviolet light with a wavelength of 2537Å (Angstroms) through the transparent window of the chip.

The integrated dose (ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²].

When the Toshiba GL-15 sterilizing lamp is used and the device is exposed at a distance of 1cm from the lamp surface, erasure will be achieved within 60 minutes.

Using a commercial lamp with an ultraviolet light intensity of 12000 [μw/cm²] reduces the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (10×60) [sec] ≅ 15 [w·sec/cm²].)

The TMM27512D's erasure begins to occur when exposed to light with wavelengths shorter than 4000Å. Sunlight and flourescent lamps both include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TMM27512D's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES(NUMBER)		$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read Operation (Ta=0~70°C)	Read	L	L	5V	Data Out	Active
	Output Deselect	*	H		High Impedance	Active
	Standby	H	*		High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	V_{PP}	6V	Data In	Active
	Program Inhibit	H	V_{PP}		High Impedance	Active
	Program Verify	L	L		Data Out	Active

Note : H ; V_{IH}, L ; V_{IL}, * ; V_{IH} or V_{IL}

READ MODE

The TMM27512D has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) controls the output buffers, independent of device selection.

Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addressess.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$=V_{IL}, and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

With $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, outputs will be in a high impedance state, so two or more TMM27512D's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27512D has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TMM27512D is placed in the standby mode which reduces 70% of the operating current. The outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27512D are in the "1" state which is the erased state. The programming operation introduces "Os" data into the desired bit locations by electrical programming.

The TMM27512D is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 12.5V and $\overline{CE}$ is at TTL-Low level

The TMM27512D can be programmed at any location, anytime, either individually, sequentially or at random.

PROGRAM VERIFY MODE

The verify mode verifies that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}/V_{PP}$ at V_{IL} and at $\overline{CE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a TTL high level $\overline{CE}$ input inhibits the TMM27512D from being programmed.

Programming of two or more TMM27512D's in parallel with different data is easily accomplished: all inputs except for $\overline{CE}$ are commonly connected, a TTL Low level program pulse is applied to the $\overline{CE}$ of the desired device only, and TTL high level signals are applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode.

This high speed programming mode is performed at V_{CC}=6.0V and $\overline{OE}/V_{PP}$=12.5V

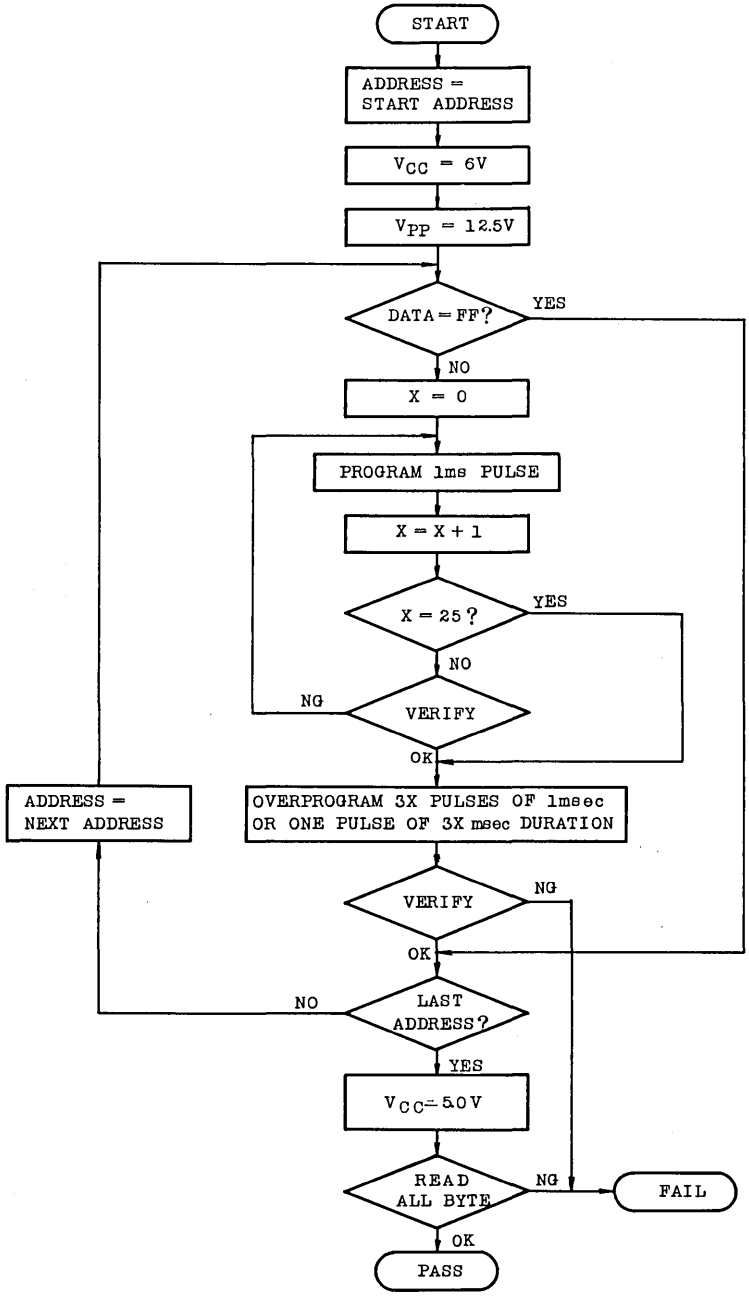
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. The programmed data is then verified by using the Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and the programmed data is reverified. This should be repeated until the programmed data is correct. (max. 25 times)

After correctly programming the selected address, an additional program pulse with width 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=5V.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TMM27512D which identifies its manufacture and device type.

The programming equipment may be used to read out the manufacturer code and device code from the TMM27512D by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output under these conditions is the manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (07).

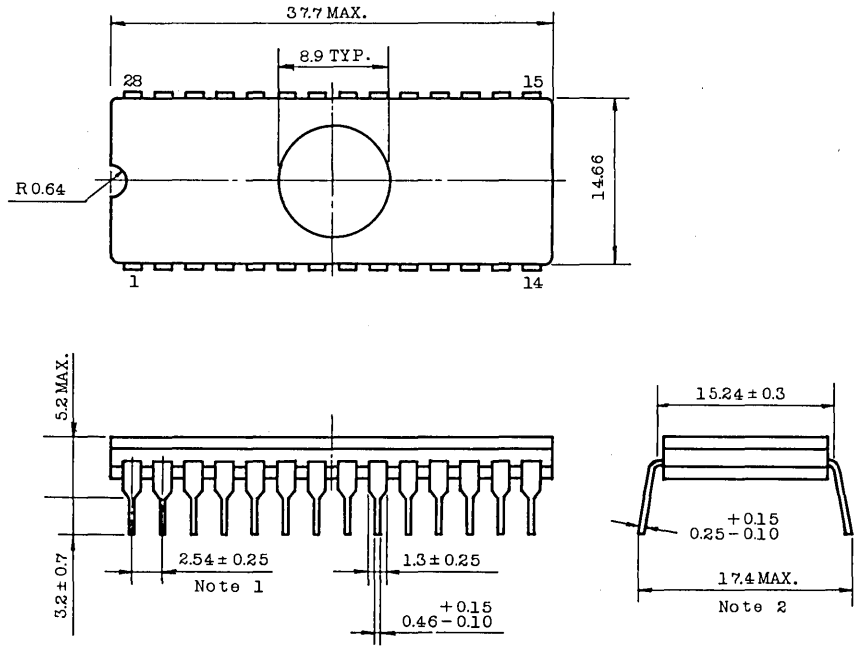
The following table shows electric signature of the TMM27512D.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	0	0	1	0	1	0	1	15

Notes : A9 = 12V±0.5V
A1~A8, A10~A15, $\overline{CE}$, $\overline{OE}$ = V_{IL}

OUTLINE DRAWINGS

Unit in mm



Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in milimeters.

Note : Toshiba does not assume any responsibility for use of any circuitry described : no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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