DATA SHEET

TDA4886
140 MHz video controller with I²C-bus

Product specification
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Philips
Semiconductors

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140 MHz video controller with I²C-bus TDA4886

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2 GENERAL DESCRIPTION

The TDA4886 is a monolithic integrated RGB pre-amplifier for colour monitor systems (e.g. 15" and 17") with I²C-bus control and OSD. In addition to bus control, beam current limiting and contrast modulation are possible. The signals are amplified in order to drive commonly used video modules or discrete solutions. Individual black level control with negative feedback from the cathode (DC coupling) or gradually adaptable black level control with positive feedback and 3 DAC outputs for external cut-off control (AC coupling) is possible.

With special advantages the circuit can be used in conjunction with the TDA485X monitor deflection IC family.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4886	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 7)		7.6	8.0	8.8	V
I_P	supply current (pin 7)		–	21	25	mA
$V_{P1,2,3}$	channel supply voltage (pins 21, 18 and 15)		7.6	8.0	8.8	V
$I_{P1,2,3}$	channel supply current (pins 21, 18 and 15)		–	21	25	mA
$V_{i(b-w)}$	input voltage (black-to-white value; pins 6, 8 and 10)		–	0.7	1.0	V
$V_{o(b-w)}$	nominal output voltage swing (black-to-white value; pins 22, 19 and 16)	nominal contrast; maximum gain	–	2.8	–	V
$V_{o(b-w)(max)}$	maximum output voltage swing (black-to-white value; pins 22, 19 and 16)	maximum contrast; maximum gain	–	4.54	–	V
V_o	output voltage level (pins 22, 19 and 16)		0.05	–	$V_P - 1$	V
$V_{bl(DC)}$	typical reference black level for DC coupling (pins 22, 19 and 16)	control bit FPOL = 0	0.5	–	2.5	V
$V_{bl(AC)}$	typical reference black level for AC coupling (pins 22, 19 and 16)	control bit FPOL = 1 and PEDST = 0				
		BLH2 = 0; BLH1 = 0	–	0.77	–	V
		BLH2 = 0; BLH1 = 1	–	1.01	–	V
		BLH2 = 1; BLH1 = 0	–	1.25	–	V
		BLH2 = 1; BLH1 = 1	–	1.49	–	V
$I_{o(sink)}$	peak output sink current	during fast signal transients	–	–	20	mA
$I_{o(source)}$	peak output source current	during fast signal transients	–40	–	–	mA
B	bandwidth	–3 dB (small signal)	–	160	–	MHz
$t_{r(o)}$	video rise time at signal outputs (pins 22, 19 and 16)		–	3.2	–	ns
$t_{f(o)}$	video fall time at signal outputs (pins 22, 19 and 16)		–	4	–	ns
dV_o	over/undershoot at signal outputs (pins 22, 19 and 16)	minimum rise/fall time	–	–	10	%
$\alpha_{ct(f)}$	crosstalk suppression by frequency	f = 50 MHz	25	–	–	dB
C_C	contrast control related to nominal contrast		–28	–	+4.2	dB
TR_o	tracking of output signals for contrast variation from maximum to minimum		–	0.0	0.5	dB
G_C	gain control related to maximum gain		–7.3	–	0	dB
BC	brightness control (typical black level voltage change related to nominal output signal amplitude)		–10	–	+30	%
$V_{o(OSD)(max)}$	maximum OSD output voltage swing related to nominal output voltage swing (pins 22, 19 and 16)	maximum OSD contrast; maximum gain	–	120	–	%
C_{OSD}	OSD contrast control related to maximum OSD contrast		–12	–	0	dB

5 BLOCK DIAGRAM

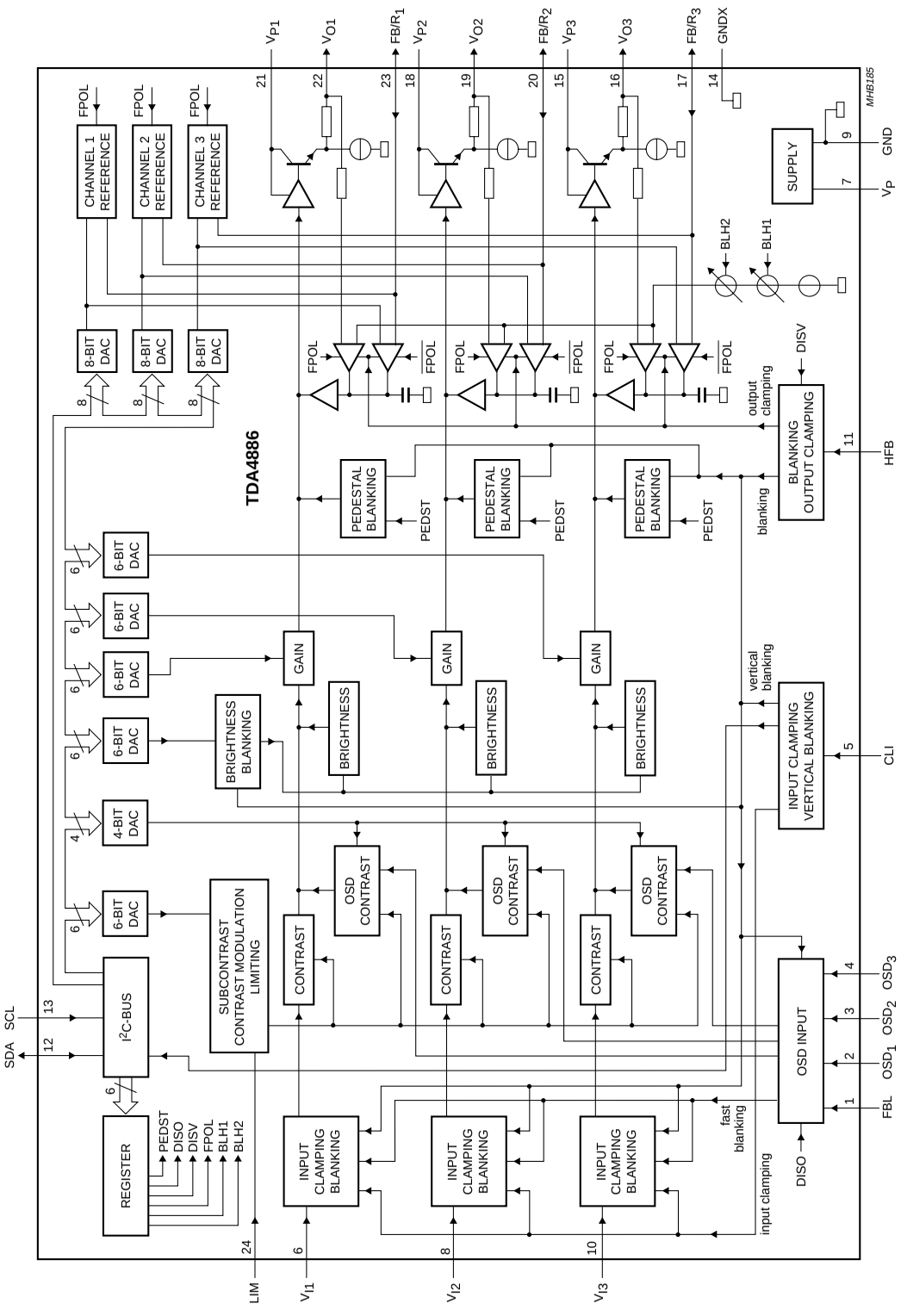


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
FBL	1	fast blanking input for OSD insertion
OSD_1	2	OSD input channel 1
OSD_2	3	OSD input channel 2
OSD_3	4	OSD input channel 3
CLI	5	input clamping; vertical blanking input
V_{I1}	6	signal input channel 1
V_P	7	supply voltage
V_{I2}	8	signal input channel 2
GND	9	ground
V_{I3}	10	signal input channel 3
HFB	11	horizontal flyback input (output clamping, blanking)
SDA	12	I²C-bus serial data input/output
SCL	13	I²C-bus clock input
GNDX	14	ground channels 1, 2 and 3
V_{P3}	15	supply voltage channel 3
V_{O3}	16	signal output channel 3
FB/R_3	17	feedback input/reference voltage output channel 3
V_{P2}	18	supply voltage channel 2
V_{O2}	19	signal output channel 2
FB/R_2	20	feedback input/reference voltage output channel 2
V_{P1}	21	supply voltage channel 1
V_{O1}	22	signal output channel 1
FB/R_1	23	feedback input/reference voltage output channel 1
LIM	24	subcontrast, contrast modulation, beam current limiting input

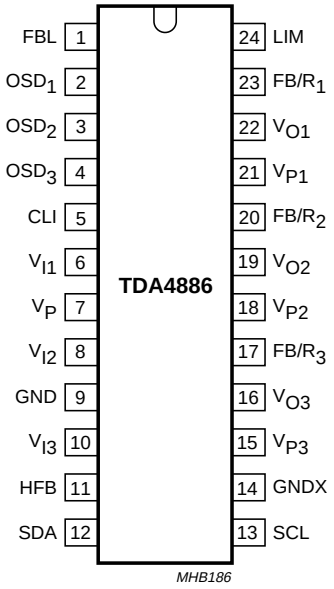


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

See block diagram (Fig.1) and definition of levels and output signals (see Chapter “Characteristics” notes 1 to 3; Figs 3 to 6).

7.1 Signal input stage (input clamping, blanking and clipping)

The RGB input signals with nominal signal amplitude of 0.7 V are capacitively coupled into the TDA4886 from a low-ohmic source (75 Ω recommended) and actively clamped to an internal DC voltage during signal black level. Because of the high-ohmic input impedance of the TDA4886 the coupling capacitor (which also functions as a storage capacitor during clamping pulses) can be relatively small (10 nF recommended). Very small input currents will discharge the coupling capacitor resulting in black output signals for missing **input clamping pulses**.

Composite signals will not disturb normal operation because a **clipping circuit** cuts all signal parts below black level.

A fast **signal blanking** stage belongs to the input stage which is driven by several **blanking pulses** (see Section “Clamping and blanking pulses”) and control bit DISV = 1. During the off condition the internal reference black level will be inserted instead of the input signals.

7.2 Electronic potentiometer stages

7.2.1 Contrast control (driven by I²C-bus, 6-bit DAC)

The input signals related to the internal reference black level can be simultaneously adjusted by contrast control with a control range of typically 32 dB. The nominal contrast setting is defined for 26H (4.2 dB below maximum).

7.2.2 Brightness control (driven by I²C-bus, 6-bit DAC)

With brightness control the video black level will be shifted in relation to the reference black level simultaneously for all three channels. With a negative setting (maximum 10% of nominal signal amplitude) dark signal parts will be lost in ultra black while for positive settings (maximum 30% of nominal signal amplitude) the background will alter from black to grey. The nominal brightness setting (10H) is no shift. The brightness setting is also valid for OSD signals. During blanking and output clamping the video black level will be blanked to reference black level (**brightness blanking**).

7.2.3 Gain control (driven by I²C-bus, 6-bit DAC) and grey scale tracking

Gain control is used for white point adjustment (correction for different voltage to light amplification of the three colour channels) and therefore individual for the three channels. The video signals related to the reference black level can be gain controlled within a range of typically 7.3 dB. The nominal setting is maximum gain. The video signal is the addition of the contrast controlled input signal and the brightness shift. The gain setting is also valid for OSD signals, thus the complete ‘grey scale’ is effected by gain control.

7.3 Output stage

In the output stage the nominal input signal will be amplified to 2.8 V output colour signal at nominal contrast and maximum gain. The maximum input to output amplification at maximum contrast and gain settings is 16.2 dB. By **output clamping** the reference black level can be adjusted. In order to achieve fast rise and fall times of the output signals with minimum crosstalk between the channels, each output stage has its own supply voltage pin.

7.4 Pedestal blanking

For the video portion the reference black level should correspond to the ‘extended cut-off voltage’ at the cathode. Nevertheless during vertical flyback retrace lines may be visible, though blanking to spot cut-off is useful. With control bit PEDST = 1 the pedestal black level will be adjusted by output clamping instead of the reference black level (see Fig.5). The pedestal black level is more negative than the video black level at minimum brightness setting and the voltage difference to reference black level is fixed.

7.5 Output clamping, feedback references and DAC outputs

The aim of the output clamping (pins FB/R_1, FB/R_2 and FB/R_3 with control bit FPOL = 0, internal feedback with control bit FPOL = 1) is to set the reference black level of the signal outputs to a value which corresponds to the ‘extended cut-off voltage’ of the CRT cathodes. With a lack of output clamping pulses the integrated storage capacitors will be discharged resulting in output signals going to switch-off voltage. Feedback references are driven by the I²C-bus.

1. **Control bit FPOL = 0**

   The cathode voltage (DC-coupled) is divided by a voltage divider and fed back to the IC. During the **output clamping pulse** it is compared with an adjustable feedback reference voltage with a range of approximately 5.77 to 4.05 V. Any difference will lead to a reference black level correction (control bit PEDST = 0) or pedestal black level correction (control bit PEDST = 1) by charging or discharging the integrated capacitor which stores the black level information between the output clamping pulses. The DC voltages of the output stages should be designed in such a way that the reference black level/pedestal black level is within the range of 0.5 to 2.5 V.

   For correct operation it is necessary that there is enough headroom for ultra black signals (negative brightness setting, pedestal black level if control bit PEDST = 1). Any clipping with the video supply voltage at the cathode can disturb the signal rise/fall times or the black level stabilization.

2. **Control bit FPOL = 1**

   For applications with AC-coupled cathodes the signal outputs are fed back internally. During the output clamping pulse they are compared with a feedback reference voltage of approximately 0.75, 1.0, 1.25 or 1.5 V (depending on the values of control bits BLH2 and BLH1). These values ensure a good adaptability to discrete and integrated post amplifiers as well.

   For black level restoration the DAC outputs (FB/R_1, FB/R_2 and FB/R_3) with a range of approximately 5.77 to 4.05 V can be used.

   The use of **pedestal blanking** allows a very simple black level restoration with a DC diode clamp instead of a complicated pulse restoration circuit because the pedestal black level is the most negative output signal.

7.6 Clamping and blanking pulses

The pin CLI of TDA4886 can be directly connected to pin CLBL of e.g. TDA4855 sync processor for input clamping pulses and vertical blanking pulses.
The threshold for the input clamping pulse (typical 3 V) is higher than the threshold for the vertical blanking pulse (typical 1.4 V) but there must be no blanking during input clamping. Thus vertical blanking only is enabled if no input clamping is detected. For this reason the input clamping pulse must have rise/fall times faster than 75 ns/V during the transition from 1.2 to 3.5 V and vice versa. The internal vertical blanking pulse will be delayed by typical 270 ns.

During the vertical blanking pulse at pin CLI **signal blanking**, **brightness blanking** and with control bit PEDST = 1 **pedestal blanking** will be activated. Input clamping pulses during vertical blanking will not switch off blanking.

For proper **input clamping** the input signals have to be at black level during the input clamping pulse.

An input pulse at pin HFB (e.g. horizontal flyback pulse) will be scanned with two thresholds. If the input pulse exceeds the first one (typical 1.4 V) **signal blanking**, **brightness blanking** and if control bit PEDST = 1 **pedestal blanking** will be activated. If the input pulse exceeds the second one (typical 3 V) additionally **output clamping** will be activated. The vertical blanking pulse can also be mixed with the horizontal flyback pulse at pin HFB.

7.7 On Screen Display (OSD)

If the fast blanking input signal at pin FBL exceeds the threshold (typical 1.4 V) the input signals are blanked (**signal blanking**) and OSD signals are enabled. Then any signal at pins OSD_1, OSD_2 or OSD_3 exceeding the same threshold will create an insertion signal with an amplitude of 120% of the nominal colour signal (approximately 74% of the maximum colour signal). The amplitude can be controlled by OSD contrast (driven by the I²C-bus) with a range of 12 dB. The OSD signals are inserted at the same point as the contrast controlled input signals and will be treated with brightness and gain control like normal input signals.

With control bit DISO = 1 OSD, signal insertion and fast blanking (pin FBL) are disabled.

7.8 Subcontrast/contrast modulation and beam current limiting

The pin LIM is a linear contrast control pin which allows subcontrast setting, contrast modulation and beam current limiting. The maximum contrast is defined by the actual I²C-bus setting. Input signals at pin LIM act on video and OSD signals and do not affect the contrast bit resolution.

To achieve brightness uniformity over the screen, scan dependent contrast modulation is possible.

7.9 I²C-bus control

The TDA4886 contains an I²C-bus receiver for several control functions:

1. Contrast control with 6-bit DAC
2. Brightness control with 6-bit DAC
3. OSD contrast control with 4-bit DAC
4. Gain control for each channel with 6-bit DAC
5. Internal feedback reference and external reference voltage control for each channel with 8-bit DAC
6. Control register with control bits BLH2, BLH1, FPOL, DISV, DISO and PEDST.

After power-up and after internal power-on reset of the I²C-bus the registers are set to the following values:

- Control bit FPOL to logic 1
- Control bits BLH2, BLH1, DISV, DISO and PEDST to logic 0
- All other alignment registers to logic 0 (minimum value for control registers).

7.10 I²C-bus data buffer

1. **Buffered mode**

   Adjustments via the I²C-bus are synchronized with vertical blanking pulse at CLI.

   a) Most significant bit (MSB) of subaddresses is set to logic 1.

   b) Only one I²C-bus transmission in buffered mode is accepted before the start of the vertical blanking pulse. Following transmission trials will get no acknowledge.

   c) Received data is stored in one internal 8-bit buffer.

   d) Adjustments will take effect with detection of the first vertical blanking pulse after the end of according I²C-bus transmission.

   e) Waiting for vertical blanking pulse in buffered mode can be interrupted by power-on reset.

   f) Auto-increment is impossible.

   g) Buffered mode should be used for user adjustments such as contrast, OSD contrast and brightness while picture on monitor is visible.

2. **Direct mode**

   Adjustments via the I²C-bus take effect immediately.

   a) Most significant bit (MSB) of subaddresses is set to logic 0.

   b) Number of I²C-bus transmissions in direct mode is unlimited.

   c) Adjustments take effect directly at the end of each I²C-bus transmission.

   d) Direct mode can be used for all adjustments but large changes of control values may appear as visual disturbances in the picture on the monitor.

   e) Auto-increment is possible.

   f) Vertical blanking pulse is not necessary.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage (pin 7)		0	8.8	V
$V_{P1, 2, 3}$	supply voltage channels 1, 2 and 3 (pins 21, 18 and 15)		0	8.8	V
V_i	input voltage (pins 6, 8 and 10)		−0.1	V_P	V
V_{ext}	external DC voltage applied to the following pins:				
	pins 1 to 4		−0.1	V_P	V
	pins 5 and 11		−0.1	V_P + 0.7	V
	pins 12 and 13		−0.1	V_P	V
	pins 23, 20 and 17		−0.1	V_P + 0.7	V
	pins 22, 19 and 16		note 1	note 1	
	pin 24		−0.1	V_P	V
$I_{o(av)}$	average output current (pins 22, 19 and 16)		−	20	mA
I_{OM}	peak output current (pins 22, 19 and 16)		−	50	mA
P_{tot}	total power dissipation		−	1400	mW
T_{stg}	storage temperature		−25	+150	°C
T_{amb}	operating ambient temperature		−20	+70	°C
T_j	junction temperature		−25	+150	°C
V_{ESD}	electrostatic handling for all pins				
	machine model	note 2	−250	+250	V
	human body model	note 3	−2000	+2000	V

Notes

1. No external voltages.
2. Equivalent to discharging a 200 pF capacitor via a 0.75 μH inductance (*"UZW-B0/FQ-B302"*).
3. Equivalent to discharging a 100 pF capacitor via a 1500 Ω series resistor (*"UZW-B0/FQ-A302"*).

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	55	K/W

10 CHARACTERISTICS

All voltages and currents are measured in a dedicated test circuit which is optimized for best high frequency performance; all voltages are measured with respect to GND (pins 9 and 14); $V_P = V_{P1, 2, 3} = 8$ V (pins 7, 21, 18 and 15); $T_{amb} = 25$ °C; nominal input signals [0.7 V (p-p) at pins 6, 8 and 10]; nominal colour signals at signal outputs (pins 22, 19 and 16); reference black level (V_{rbl}) approximately 0.77 V; nominal settings for brightness and contrast; maximum settings for OSD contrast and gain; no subcontrast, modulation of contrast or limiting ($V_{24} \geq 5$ V); no OSD fast blanking (pin 1 connected to ground); notes 1 to 3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage (pin 7)		7.6	8.0	8.8	V
I_P	supply current (pin 7)	note 4	–	21	25	mA
$V_{P1,2,3}$	channel supply voltage (pins 21, 18 and 15)		7.6	8.0	8.8	V
$I_{P1,2,3}$	channel supply current (pins 21, 18 and 15)	signal outputs (pins 22, 19 and 16) open-circuit; $V_{rbl} \approx 0.77$ V; notes 4 and 5	–	21	25	mA
V_{PSO}	supply voltage for signal switch off (threshold at pin 7)	signal outputs switched to switch-off voltage	–	–	7.2	V
Input clamping and vertical blanking input, validation of buffered I²C-bus data (pin 5)						
V_5	input clamping and vertical blanking input signal	notes 6 and 7				
		no vertical blanking, no input clamping	–0.1	–	+1.2	V
		vertical blanking, no input clamping	1.6	–	2.6	V
		input clamping, no vertical blanking	3.5	–	V_P	V
I_5	input current	$V_5 = 1$ V	–	–0.2	–	µA
		pin 5 connected to ground; note 8	–80	–60	–30	µA
		$V_5 = -0.1$ V; note 8	–250	–200	–100	µA
$t_{r/f5}$	rise/fall time for input clamping pulse, disable for vertical blanking	note 6; see Fig.7	–	–	75	ns/V
t_{W5}	width of input clamping pulse		0.6	–	–	µs
t_{W5I2C}	width of vertical blanking pulse for validation of buffered I²C-bus data	leading and trailing edge threshold $V_5 = 1.4$ V; note 7	10	–	–	µs
$t_{I2Cvalid}$	delay between leading edge of vertical blanking pulse and validation of buffered I²C-bus data	I²C-bus transmission in buffered mode completed; leading edge threshold $V_5 = 1.4$ V; note 7	–	–	2	µs
$t_{I2Cdead}$	dead time of I²C-bus receiver after synchronizing vertical blanking pulse in case of a completed I²C-bus transmission in buffered mode	leading edge threshold $V_5 = 1.4$ V; note 7	15	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{dl5}	delay between leading edges of vertical blanking input pulse and signal blanking at signal outputs	V_{11} < 0.8 V; input pulse with 50 ns/V; threshold for rising input pulse V_5 = 1.4 V; threshold after input clamping pulse V_5 = 3 V; $V_{I(b\text{-}w)}$ = 0.7 V; see Fig.7	–	270	–	ns
t_{dt5}	delay between trailing edges of vertical blanking input pulse and internal blanking pulse	V_{11} < 0.8 V; input pulse with 50 ns/V; threshold V_5 = 1.4 V; see Fig.7	–	115	–	ns
Output clamping and blanking input (pin 11)						
V_{11}	output clamping and blanking input signal	note 9				
		no blanking, no output clamping	–0.1	–	+0.8	V
		blanking, no output clamping	2.0	–	2.6	V
		blanking, output clamping	3.5	–	V_P	V
I_{11}	input current	V_{11} = 0.8 V	–	–0.4	–	µA
		pin 11 connected to ground; note 8	–80	–60	–30	µA
		V_{11} = –0.1 V; note 8	–250	–200	–100	µA
t_{W11}	width of output clamping pulse	threshold V_{11} = 3 V	1	–	–	µs
Video signal inputs (channel 1: pin 6; channel 2: pin 8; channel 3: pin 10)						
$V_{i(b\text{-}w)6,8,10}$	positive input signal referred to black		–	0.7	1.0	V
$I_{I6,8,10}$	DC input current	no input clamping; $V_{I6,8,10} = V_{I(clamp)6,8,10}$; T_{amb} = –20 to +70 °C	0.02	0.20	0.35	µA
		during input clamping; $V_{I6,8,10} = V_{I(clamp)6,8,10}$ ±0.7 V	±100	±135	±170	µA
Signal blanking						
$\alpha_{ct(blank)}$	crosstalk suppression from input to output during blanking	control bit DISV = 1; f = 80 MHz	20	–	–	dB
		control bit DISV = 1; f = 120 MHz	10	–	–	dB
Clipping of negative input signals (measured at signal outputs)						
ΔV_{clipp}	offset during sync clipping related to nominal colour signal	$V_{I6,8,10} = V_{I(clamp)6,8,10}$; note 10; see Fig.3	–	–	2	%
Contrast control; see Fig.8 and note 11						
d_C	colour signal related to nominal colour signal	3FH (maximum)	–	4.2	–	dB
		26H (nominal)	–	0	–	dB
		00H (minimum)	–	–28	–	dB
ΔG_{track}	tracking of output colour signals of channels 1, 2 and 3	3FH to 00H; note 12	–	0.0	0.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fast blanking (pin 1) and OSD signal insertion (channel 1: pin 2; channel 2: pin 3; channel 3: pin 4); note 13						
V_1	fast blanking input signal	no video signal blanking, OSD signal insertion disabled	0	–	1.1	V
		video signal blanking, OSD signal insertion enabled	1.7	–	V_P	V
$V_{2,3,4}$	OSD input signal	V_1 > 1.7 V				
		no internal OSD signal insertion	0	–	1.1	V
		internal OSD signal insertion	1.7	–	V_P	V
$t_{r(OSD)}$	rise time of OSD colour signals (pins 22, 19 and 16)	10 to 90% amplitude; input pulse with 1.2 ns/V	–	–	4	ns
$t_{f(OSD)}$	fall time of OSD colour signals (pins 22, 19 and 16)	90 to 10% amplitude; input pulse with 1.2 ns/V	–	–	7	ns
$t_{g(CO)}$	width of (negative going) OSD signal insertion glitch, leading edge (pins 22, 19 and 16)	identical pulses at fast blanking input (pin 1) and OSD signal inputs (pins 2, 3 and 4)	0	–	6	ns
$t_{g(OC)}$	width of (negative going) OSD signal insertion glitch, trailing edge (pins 22, 19 and 16)	identical pulses at fast blanking input (pin 1) and OSD signal inputs (pins 2, 3 and 4)	0	–	6	ns
dV_{OSD}	overshoot/undershoot of OSD colour signal related to actual OSD output pulse amplitude (pins 22, 19 and 16)	pulse with 1.2 ns/V at OSD signal inputs (pins 2, 3 and 4)	–	–	10	%
$V_{OSD(max)}$	maximum OSD colour signal related to nominal colour signal (pins 22, 19 and 16)	maximum OSD contrast; maximum gain	100	120	140	%
OSD contrast control; see Fig.9 and note 14						
d_{OC}	OSD colour signal related to maximum OSD colour signal	0FH (maximum)	–	0	–	dB
		00H (minimum)	–14	–12	–10	dB
Subcontrast/contrast modulation and beam current limiting (pin 24); see Fig.8 and note 15						
$V_{24(nom)}$	nominal input voltage	pin 24 open-circuit	4.7	5.0	5.3	V
$V_{24(start)}$	starting voltage for contrast and OSD contrast reduction		4.2	4.5	4.8	V
$V_{24(stop)}$	stop voltage for contrast and OSD contrast reduction	–32 dB below maximum colour signal (contrast setting 3FH)	1.5	2.0	2.5	V
B_{24}	bandwidth of contrast modulation	–3 dB	4	–	–	MHz
$I_{24(max)}$	maximum input current	V_{24} = 0 V	–1.0	–	–	μA
Brightness control; see Fig.10 and notes 16 and 17						
ΔV_{bl}	difference between black level and reference black level at signal outputs related to nominal colour signal	3FH (maximum)	25	30	35	%
		10H (nominal)	–	0	–	%
		00H (minimum)	–12	–10	–8	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Gain control; see Fig.11 and note 18						
d_G	video signal related to video signal at maximum gain	3FH (maximum)	–	0	–	dB
		00H (minimum)	–8.3	–7.3	–6.3	dB
Pedestal blanking						
$\Delta V_{22,19,16(PED)}$	difference from pedestal black level to video black level at nominal brightness, measured at signal output pins related to nominal colour signal	note 19; see Fig.5	–18	–16	–14	%
Signal outputs (channel 1: pin 22; channel 2: pin 19; channel 3: pin 16)						
$V_{22,19,16(nom)}$	nominal colour signal	nominal contrast; maximum gain; $V_{i(b-w)}$ = 0.7 V; without load	2.5	2.8	3.1	V
$V_{22,19,16(max)}$	maximum colour signal	maximum contrast; maximum gain; $V_{i(b-w)}$ = 0.7 V; without load	4.1	4.54	5	V
$V_{22,19,16(min)}$	switch-off voltage (minimum output voltage level)		–	0.05	0.1	V
$V_{22,19,16(top)}$	maximum output voltage level	at arbitrary input signals, contrast, brightness and gain adjustments; without load	V_P – 2	–	V_P – 1	V
$R_{(o)22,19,16}$	output resistance		–	75	–	Ω
$I_{22,19,16(source)}$	maximum source current		–15	–	–	mA
$I_{22,19,16(M)(source)}$	peak source current	during fast positive signal transients	–40	–	–	mA
$I_{22,19,16(sink)}$	maximum sink current (built-in current source)	output voltage $V_{22,19,16} \approx 0.77$ V; note 20	3.2	4	–	mA
		output voltage $V_{22,19,16}$ = 6 V; note 20	1.6	2	–	mA
$I_{22,19,16(M)(sink)}$	peak sink current	during fast negative signal transients	–	–	20	mA
S/N	signal-to-noise ratio	note 21	44	–	–	dB
$D_{22,19,16(th)}$	output thermal distortion	note 22	–	–	0.6	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Frequency response at signal outputs (channel 1: pin 22; channel 2: pin 19; channel 3: pin 16)						
$\Delta G_{22,19,16(f)}$	amplification decrease by frequency response	f = 160 MHz; $V_{i(b-w)} \leq 0.2$ V (small signal)	–	1.2	3.0	dB
$t_{r(22,19,16)}$	rise time of fast transients	input rise time = 1 ns; 10 to 90% amplitude; nominal colour signal; note 23	–	3.2	3.5	ns
$t_{f(22,19,16)}$	fall time of fast transients	input fall time = 1 ns; 90 to 10% amplitude; nominal colour signal; note 23	–	4.0	4.3	ns
$dV_{22,19,16}$	over/undershoot of output signal pulse related to actual output pulse amplitude	input rise/fall time = 1 ns; nominal colour signal	–	–	10	%
Crosstalk at signal outputs (channel 1: pin 22; channel 2: pin 19; channel 3: pin 16)						
$\alpha_{ct(tr)}$	transient crosstalk suppression	input rise/fall time = 1 ns; note 24	10	–	–	dB
$\alpha_{ct(f)}$	crosstalk suppression by frequency	f = 50 MHz	25	–	–	dB
		f = 100 MHz	10	–	–	dB
Internal feedback reference voltage; see Fig.12 and note 25						
$V_{ref(n)}$	internal reference voltage for negative feedback polarity	FFH (minimum); FPOL = 0	3.85	4.05	4.2	V
		00H (maximum); FPOL = 0	5.6	5.77	5.9	V
$V_{ref(p)}$	internal reference voltage for positive feedback polarity	FPOL = 1				
		BLH2 = 0; BLH1 = 0	0.71	0.77	0.83	V
		BLH2 = 0; BLH1 = 1	0.95	1.01	1.07	V
		BLH2 = 1; BLH1 = 0	1.19	1.25	1.31	V
		BLH2 = 1; BLH1 = 1	1.43	1.49	1.55	V
Output clamping, feedback inputs for DC coupling (channel 1: pin 23; channel 2: pin 20; channel 3: pin 17)						
$I_{23,20,17(max)}$	maximum input current	during output clamping; $V_{11} > 3.5$ V; $V_{23,20,17} = 0.5$ V; FPOL = 0	–500	–200	–60	nA
$V_{22,19,16(rbl)(min)}$	minimum reference black level	PEDST = 0; $V_{11} > 3.5$ V; FPOL = 0	0.01	0.1	0.5	V
	minimum pedestal black level	PEDST = 1; $V_{11} > 3.5$ V; FPOL = 0	0.01	0.1	0.5	V
$V_{22,19,16(rbl)(max)}$	maximum reference black level	PEDST = 0; $V_{11} > 3.5$ V; FPOL = 0	2.4	2.8	–	V
	maximum pedestal black level	PEDST = 1; $V_{11} > 3.5$ V; FPOL = 0	2.4	2.8	–	V
$\Delta V_{bl(CRT)}$	black level variation at CRT	FPOL = 0; note 26	–	–	200	mV
$\Delta V_{22,19,16(bl)(lf)}$	black level variation between clamping pulses related to nominal colour signal	FPOL = 0; line frequency = 60 kHz; 10% duty cycle	–	0.25	0.5	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output clamping for AC coupling (internal feedback of signal outputs)						
$V_{22,19,16(rbl)}$	reference black level	V_{11} > 3.5 V; FPOL = 1; PEDST = 0				
		BLH2 = 0; BLH1 = 0	0.71	0.77	0.83	V
		BLH2 = 0; BLH1 = 1	0.95	1.01	1.07	V
		BLH2 = 1; BLH1 = 0	1.19	1.25	1.31	V
		BLH2 = 1; BLH1 = 1	1.43	1.49	1.55	V
	pedestal black level	V_{11} > 3.5 V; FPOL = 1; PEDST = 1				
		BLH2 = 0; BLH1 = 0	0.71	0.77	0.83	V
		BLH2 = 0; BLH1 = 1	0.95	1.01	1.07	V
		BLH2 = 1; BLH1 = 0	1.19	1.25	1.31	V
		BLH2 = 1; BLH1 = 1	1.43	1.49	1.55	V
$\Delta V_{22,19,16(bl)(lf)}$	black level variation between clamping pulses related to nominal colour signal	FPOL = 1; line frequency = 60 kHz; 10% duty cycle	–	0.25	0.5	%
External reference voltages for AC coupling (FB/R_1: pin 23; FB/R_2: pin 20; FB/R_3: pin 17); see Fig.13 and note 27						
$V_{23,20,17}$	external reference voltage	FFH (minimum); FPOL = 1	3.85	4.05	4.2	V
		00H (maximum); FPOL = 1	5.6	5.77	5.9	V
$R_{23,20,17}$	output resistance	FPOL = 1	–	100	–	Ω
$I_{23,20,17(sink)}$	maximum sink current	FPOL = 1	–	–	400	μA
$I_{23,20,17(source)}$	maximum source current	FPOL = 1	–	–330	–280	μA
I²C-bus inputs (SDA: pin 12; SCL: pin 13); note 28						
f_{SCL}	SCL clock frequency		–	–	100	kHz
V_{IL}	LOW-level input voltage		0.0	–	1.5	V
V_{IH}	HIGH-level input voltage		3.0	–	5.0	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	–10	–	–	μA
I_{IH}	HIGH-level input current	V_{IH} = 5 V	–10	–	–	μA
V_{OL}	LOW-level output voltage	during acknowledge	0.0	–	0.4	V
$I_{12(ack)}$	output current at pin 12 during acknowledge	V_{OL} = 0.4 V	3.0	–	5.0	mA
$V_{th(POR)(r)}$	threshold for power-on reset on	rising supply voltage	–	1.5	2.0	V
		falling supply voltage	–	3.5	–	V
$V_{th(POR)(f)}$	threshold for power-on reset off	rising supply voltage	–	–	7.0	V
		falling supply voltage	–	1.5	–	V

Notes to the characteristics

1. Definition of levels (see Figs 3 to 5)

   Reference black level: this is the level to which the input level is clamped during the input clamping pulse (V_5 > 3.5 V). It is used internally as a reference for the gain settings. It can be observed on the outputs:

   a) When the input is at black and the brightness setting is nominal (subaddress 01H = 10H)

   b) During output blanking/clamping (V_{11} > 3.5 V) if control bit PEDST = 0.

   Video black level: this is the black level of the actual video. On the input it is still equal to the reference black level. On the output it may deviate from it according to the brightness setting. Contrast setting leaves the video black level unaltered. Gain setting biases the video black level due to its influence on brightness. This is important for correct grey scale tracking.

   Pedestal black level: this is an ultra black level which deviates from reference black level by a fixed amount. It can be observed on the output during output blanking/clamping (V_{11} > 3.5 V) if control bit PEDST = 1.

   Switch-off voltage: this is the lowest signal voltage at outputs. The signals will be switched off by discharging the internal black level storage capacitors if the supply voltage is less than V_{PSO}.

   Blanking level: this level equals reference black (control bit PEDST = 0) or pedestal black (control bit PEDST = 1).

2. Explanation to black level adjustment:

   The three reference black levels are aligned correctly when they are made equal to the ‘extended cut-off levels’ of the three cathodes. Full raster and spot cut-off can only be achieved by enabling the pedestal blanking or by applying a negative pulse to the control grid G1.

   Negative feedback for DC-coupled cathodes (control bit FPOL = 0): the actual blanking level on the outputs depends on the external feedback application for output clamping. The loop will function correctly only if it is within the control range of $V_{22,19,16(rbl)(min)}$ to $V_{22,19,16(rbl)(max)}$. It should be noted that changing control bit PEDST in a given application will not affect the blanking level, but instead shifts the video (and needs re-alignment of the three black levels).

   Positive feedback for AC-coupled cathodes (control bit FPOL = 1): the feedback loop for output clamping is closed internally. The actual blanking level at the outputs depends on control bits BLH2 and BLH1 only. Four discrete blanking levels between approximately 0.75 and 1.5 V can be chosen. It should be noted that changing control bit PEDST will not affect the blanking level selected by control bits BLH2 and BLH1, but instead shifts the video (and needs re-alignment of the three black levels).

3. Definition of output signals (see Fig.6):

   Colour signal: all positive voltages referred to black level at signal outputs.

   Nominal colour signal: colour signal with nominal input signal (0.7 $V_{b\text{-}w}$), nominal contrast setting and maximum gain setting.

   Video signal: all positive voltages referred to reference black level at signal outputs. The video signal is the superimposing of the brightness information (ΔV_{bl}) and the colour signal.

4. The total supply current $I_P = I_7 + I_{21} + I_{18} + I_{15}$ depends on the supply voltage with a factor of approximately 4.4 mA/V and varies in the temperature range from −20 to +70 °C by approximately ±5% ($V_{22,19,16}$ = 0.77 V).

5. The channel supply current depends on the signal output current, the channel supply voltage and the signal output voltage. With $I_{px} = I_{21,18,15}$ at $V_{P1,2,3}$ = 8 V and $V_{22,19,16}$ = 0.77 V:

$$I_{21,18,15} \approx I_{px} + I_{22,19,16} + 4.4\ \frac{mA}{V} \times (V_{P1,2,3} - 8\ V) - 1\ \frac{mA}{V} \times (V_{22,\,19,\,16} - 0.77\ V)$$

6. Pin 5 should be used for input clamping and blanking during vertical retrace (signal blanking, brightness blanking and if control bit PEDST = 1 pedestal blanking). With a fast clamping pulse (transition between V_5 = 1.2 to 3.5 V and vice versa in less than 75 ns/V) no blanking will occur during input clamping.

   For 75 ns/V < $t_{r/f5} \leq$ 280 ns/V the generation of the internal vertical blanking pulse is uncertain. For $t_{r/f5}$ > 280 ns/V the internal blanking pulse will be generated.

   Pin 5 open-circuited will activate permanent input clamping and undefined blanking.

7. Pin 5 can be used to synchronize all adjustments via the I²C-bus (one by one). In case of a completed I²C-bus transmission in buffered mode only the leading edge of a vertical blanking pulse activates an adjustment. See also Section 7.10.

   After the adjustment has been activated (validation of buffered I²C-bus data) the I²C-bus will be reset and further transmissions in direct or buffered mode are enabled.

   I²C-bus transmissions in direct mode need no synchronization pulses.

8. Input voltages less than −0.1 V can produce internal substrate currents which disturb the leakage currents at the signal inputs. An internal protection circuit creates a current for pin voltages of approximately 0 V or less. Feeding clamping/blanking pulses via a resistor of some kΩ protects the pin from negative voltages.

9. Pin 11 should be used for output clamping and/or blanking. Pin 11 open-circuited will activate permanent blanking and output clamping.

10. Composite signals will not disturb normal operations because an internal clipping circuit cuts all signal parts below input reference black level (see Fig.3).

11. Contrast control acts on internal colour signals under I²C-bus control; subaddress 02H (bit resolution 1.6% of contrast range).

12. $$\Delta G_{track} = 20 \times \text{maximum of } \left\{ \left| \log\left(\frac{A_1}{A_{10}} \times \frac{A_{20}}{A_2} \right) \right| ; \left| \log\left(\frac{A_1}{A_{10}} \times \frac{A_{30}}{A_3} \right) \right| ; \left| \log\left(\frac{A_2}{A_{20}} \times \frac{A_{30}}{A_3} \right) \right| \right\} \text{dB}$$

    A_n: colour signal output amplitude in channel n = 1, 2 or 3 at any contrast setting.

    A_{n0}: colour signal output amplitude in channel n = 1, 2 or 3 at nominal contrast setting and same gain setting.

13. When OSD fast blanking is active and $V_{2,3,4}$ are HIGH (V_1 > 1.7 V, $V_{2,3,4}$ > 1.7 V) the OSD colour signals will be inserted in front of the gain potentiometers. This assures a correct grey scale of all video signals. The amplitudes of the inserted OSD signals can be controlled simultaneously by OSD contrast via the I²C-bus.

14. OSD contrast control acts on inserted OSD colour signals under I²C-bus control; subaddress 03H (bit resolution 6.7% of OSD contrast range).

15. This pin can be used for subcontrast setting, beam current limiting and contrast modulation. Both the video and OSD contrast are reduced simultaneously (see Figs 8 and 9). Because of the high-ohmic input impedance the pin should be tied to a voltage of more than 5 V or applied with a capacitor of some nF if not used.

16. Brightness control adds an I²C-bus controlled DC offset to the internal colour signal; subaddress 01H (bit resolution 1.6% of brightness range).

17. The voltage difference between video black level and reference black level is related to the colour signal (see note 3) with nominal 0.7 V (p-p) input signal, at nominal contrast (subaddress 02H = 26H) and for any gain setting.
    The voltage difference (in Volts) is proportional to the gain setting (grey scale tracking). Therefore ΔV_{bl} (in percent) is constant for any gain setting. The given values of ΔV_{bl} are valid only for video black levels higher than the signal output switch-off voltage $V_{22,19,16(min)}$.

18. Gain control acts on video signals and inserted OSD video signals under I²C-bus control; subaddress 04H (channel 1), 05H (channel 2) and 06H (channel 3; bit resolution 1.6% of gain range respectively).

19. Pedestal blanking produces an ultra black level during blanking and output clamping which is the most negative signal at the signal output pins. The reference black level which should correspond to the 'extended cut-off voltage' at the cathodes is approximately $\Delta V_{22,19,16(PED)}$ higher (see Fig.5). The use of **pedestal blanking** with AC-coupled cathodes (control bit FPOL = 1) allows a very simple black level restoration with a DC diode clamp instead of a complicated pulse restoration circuit.
20. DC load currents of signal outputs must not exceed maximum sink currents, otherwise signal distortions may occur.
21. The signal-to-noise ratio is calculated by the formula (range 1 to 120 MHz):

$$\frac{S}{N} = 20 \times \log \frac{\text{peak-to-peak value of the nominal signal output voltage}}{\text{RMS value of the noise output voltage}} \text{ dB}$$

22. Large output currents e.g. $I_{22,19,16(M)(source)}$ lead to signal depending power dissipation in output transistors. Thermal V_{BE} variation is compensated.
23. Following formula can be used to approximately determine the output rise/fall time for any other input rise/fall time:

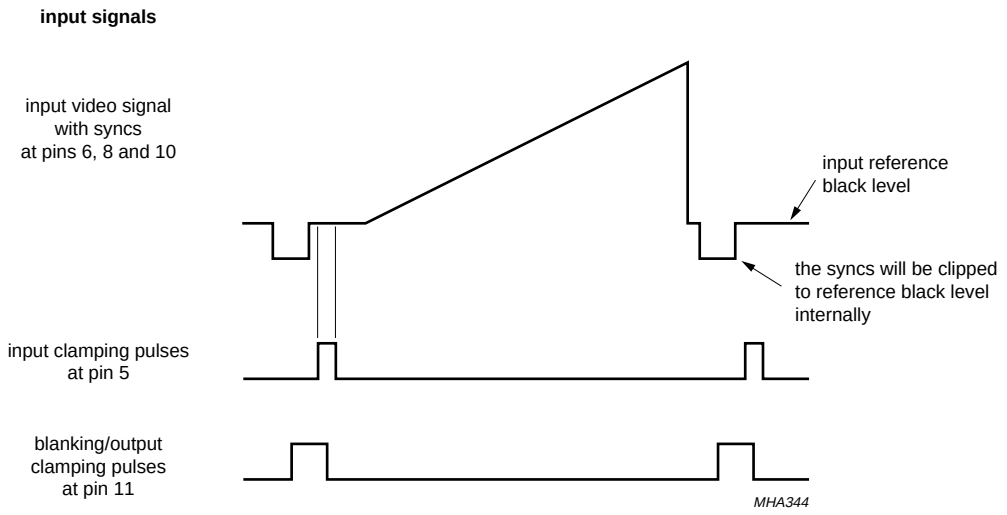
$$t^2_{r/f,\ measured} = t^2_{r/f\ (22,19,16)} + \left(t^2_{r/f,\ input} - (1\text{ns})^2 \right)$$

24. Transient crosstalk between any two output pins:
    a) **Input conditions**: any channel (channel A) with nominal input signal and 1 ns rise time. The inputs of the other two channels are capacitively coupled to ground (channel B). Gain setting to maximum (3FH). Contrast setting to nominal (26H). No limiting/modulation of contrast ($V_{24} \geq 5$ V)
    b) **Output conditions**: black level set to approximately 0.77 V for each channel at signal outputs. Output signals are V_A and V_B respectively
    c) **Transient crosstalk suppression**: $\alpha_{ct(tr)} = 20 \times \log \frac{V_A}{V_B}$ dB
25. The internal feedback reference voltages are not influenced by the value of control bit PEDST but depend on the individual adjustments via the I²C-bus, the selected feedback polarity (control bit FPOL = 0 or 1) and the selected black level for positive feedback polarity (control bit FPOL = 1 and control bits BLH2 = 0 or 1 and BLH1 = 0 or 1):

    Control bit FPOL = 0: the internal feedback reference voltage acts under I²C-bus control; subaddress 07H (channel 1), 08H (channel 2) and 09H (channel 3; bit resolution 0.4% of voltage range). Rising values of the data bytes, e.g. 00H to FFH, correspond to rising values of the resulting reference black levels at signal outputs (pins 22, 19 and 16). The internal feedback reference voltages can be measured at feedback inputs (pins 23, 20 and 17) during output clamping ($V_{11} > 3.5$ V) in closed feedback loop. The feedback loop remains operative at reference black levels between the specified values of $V_{22,19,16(rbl)(min)}$ and $V_{22,19,16(rbl)(max)}$.

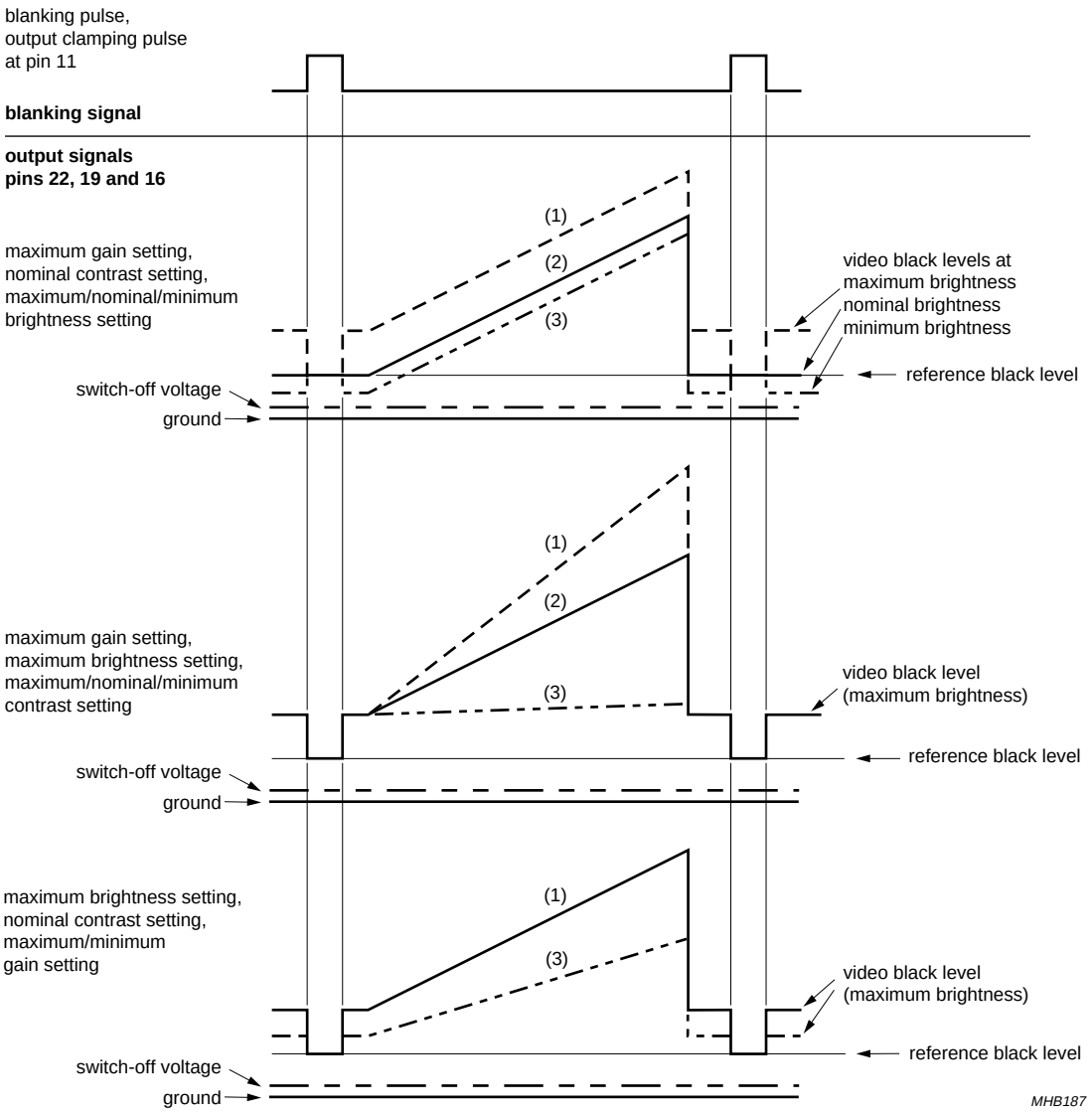
    Control bit FPOL = 1: the internal feedback reference voltage can be measured at signal outputs (pins 22, 19 and 16) during output clamping ($V_{11} > 3.5$ V). By means of control bits BLH2 and BLH1 it is possible to choose one of the four specified values between approximately 0.75 and 1.5 V. This facilitates the adaption to different kinds of post amplifiers.
26. Slow variations of video supply voltage V_{CRT} will be suppressed at the CRT cathode by the clamping feedback loop. A change of V_{CRT} with 5 V leads to a specified change of the cathode voltage.
27. The external reference voltages act under I²C-bus control for control bit FPOL = 1; subaddress 07H (FB/R_1), 08H (FB/R_2) and 09H (FB/R_3; bit resolution 0.4% of voltage range).
28. All adjustments via the I²C-bus can be synchronized with vertical blanking pulse at pin CLI. This is called I²C-bus transmission in buffered mode. The adjustments via the I²C-bus will take effect immediately in the so called direct mode.

    The timing of I²C-bus transmissions in buffered mode is related to the vertical blanking. See specification of pin 5 (vertical blanking input) and note 7.



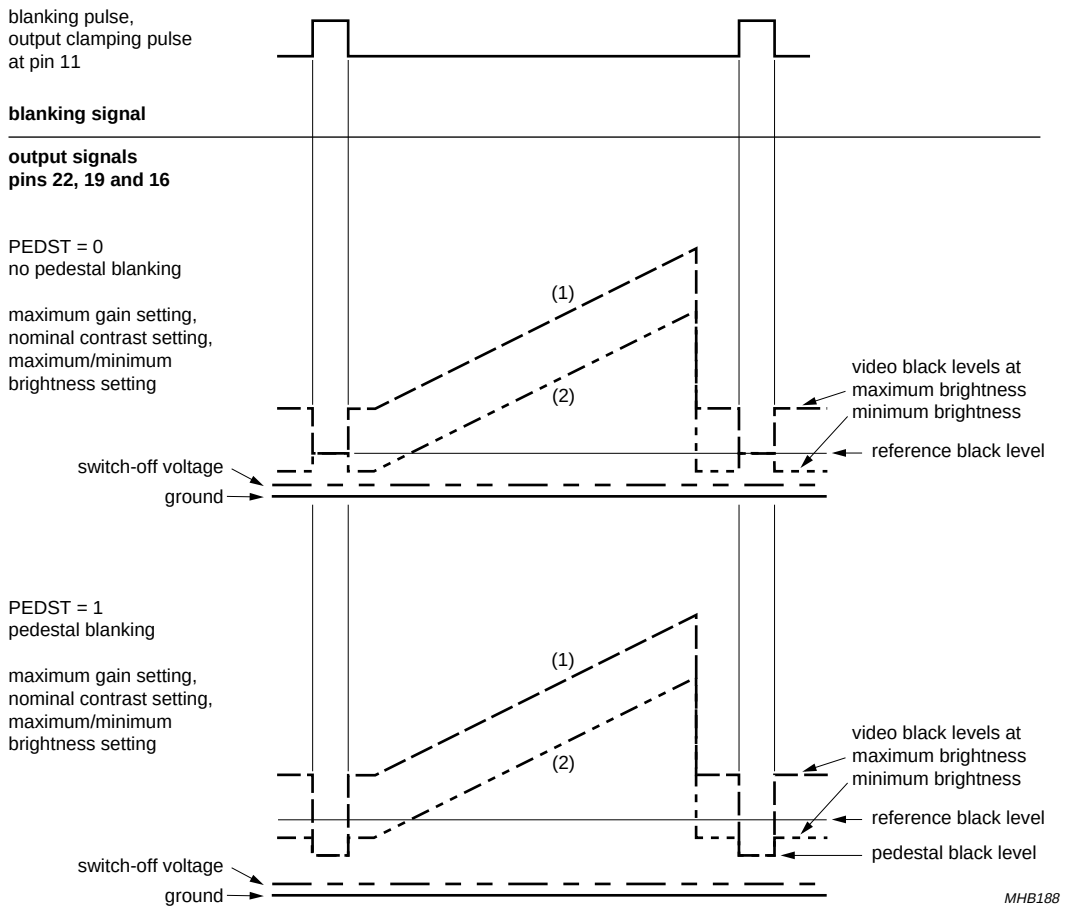
The input video signals have to be on black level during input clamping.

Fig.3 Input signals.



(1) Maximum.
(2) Nominal.
(3) Minimum.

Fig.4 Definition of levels, function of brightness setting, contrast setting, gain setting, no pedestal blanking (PEDST = 0).



(1) Maximum.
(2) Minimum.

Fig.5 Output signals without (PEDST = 0) and with pedestal blanking (PEDST = 1).

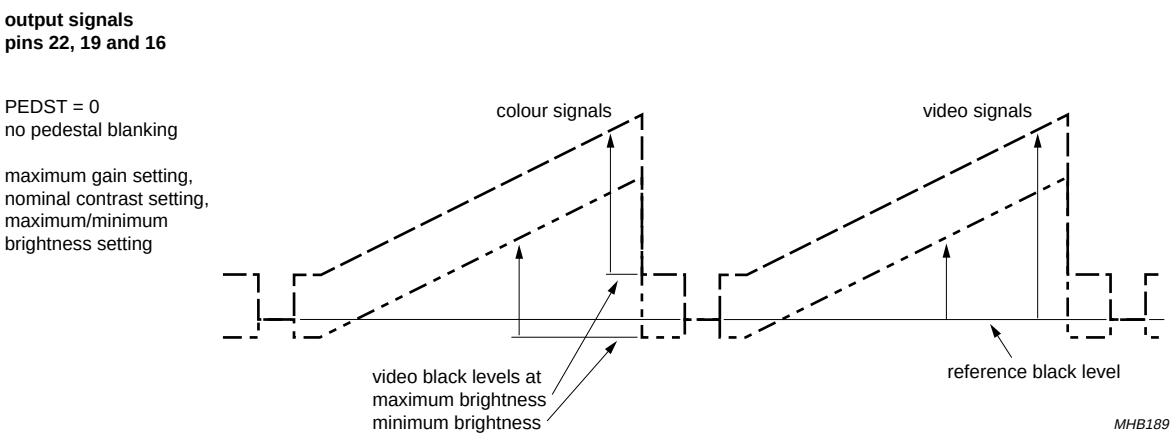


Fig.6 Definition of output signals.

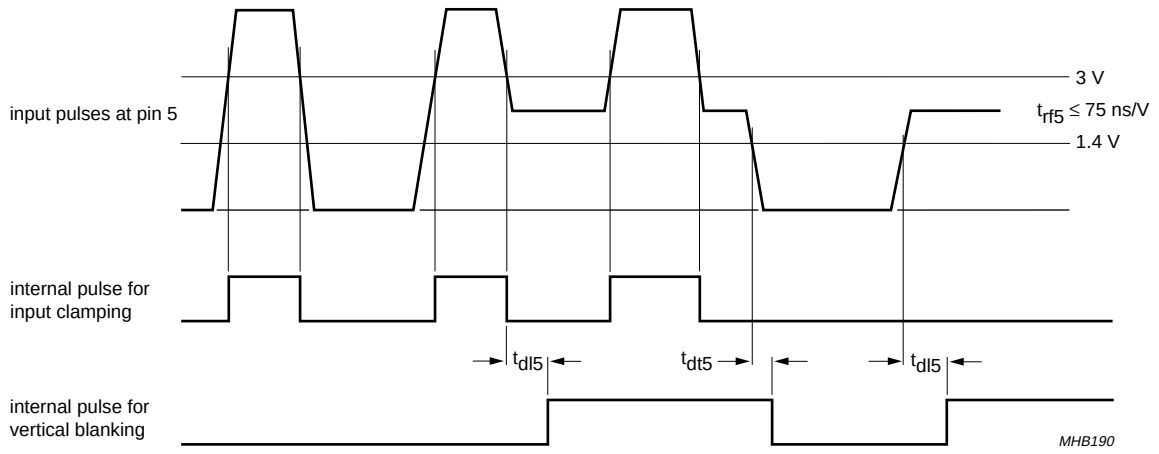
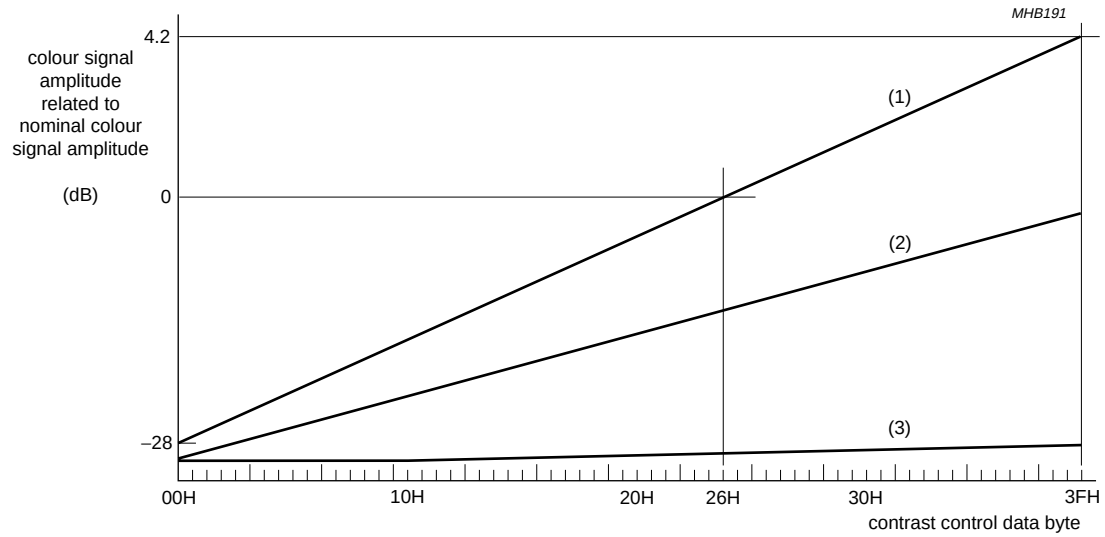
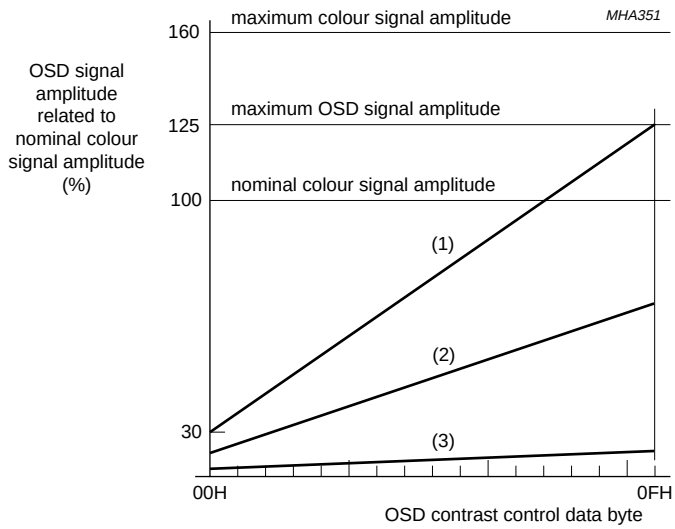


Fig.7 Timing of pulses at pin 5 and derived internal pulses.



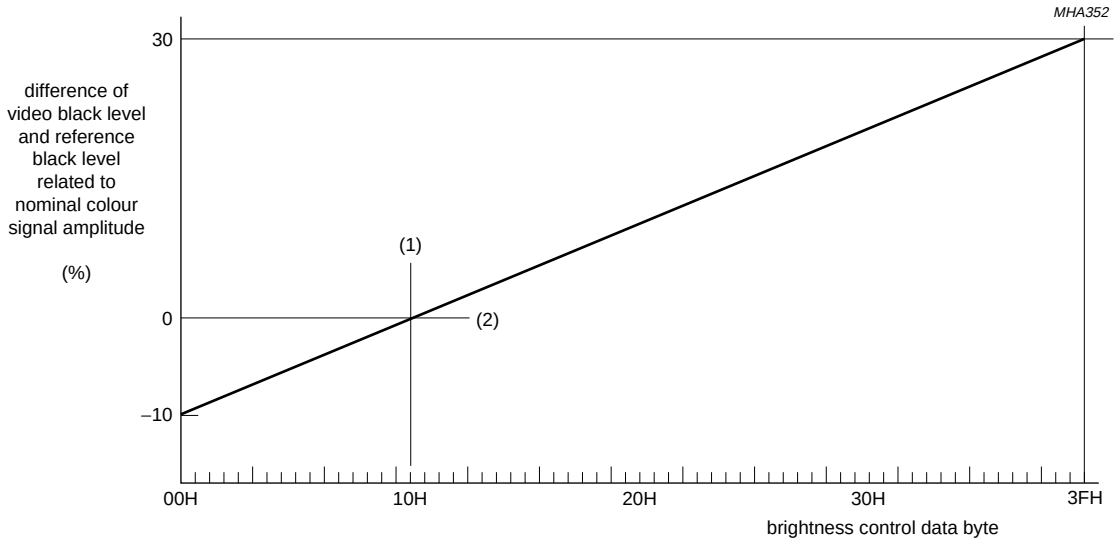
(1) No contrast reduction by subcontrast.
(2) Partial contrast reduction by subcontrast.
(3) Full contrast reduction by subcontrast.

Fig.8 Contrast control characteristic with subcontrast (equal to contrast modulation and limiting).



(1) No OSD contrast reduction by subcontrast.
(2) Partial OSD contrast reduction by subcontrast.
(3) Full OSD contrast reduction by subcontrast.

Fig.9 OSD contrast control characteristic with subcontrast (equal to contrast modulation and limiting).



(1) Nominal adjustment.
(2) Nominal brightness reference black level.

Fig.10 Brightness control characteristic.

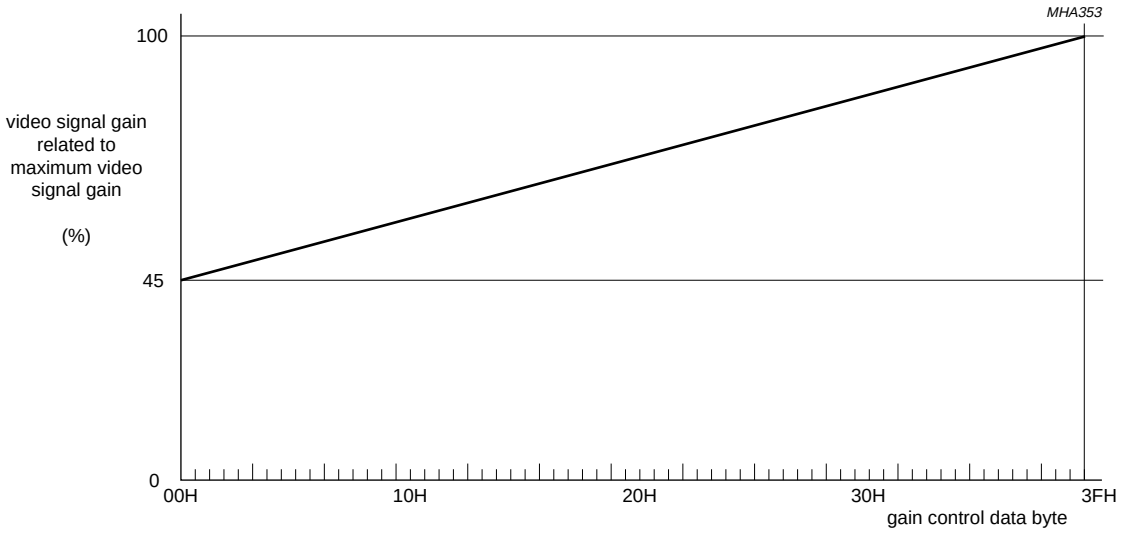
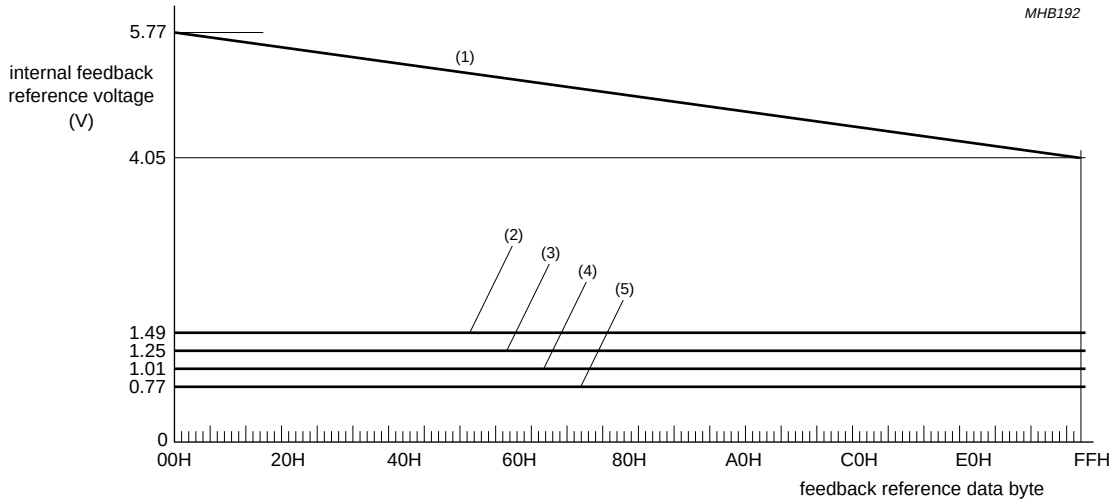
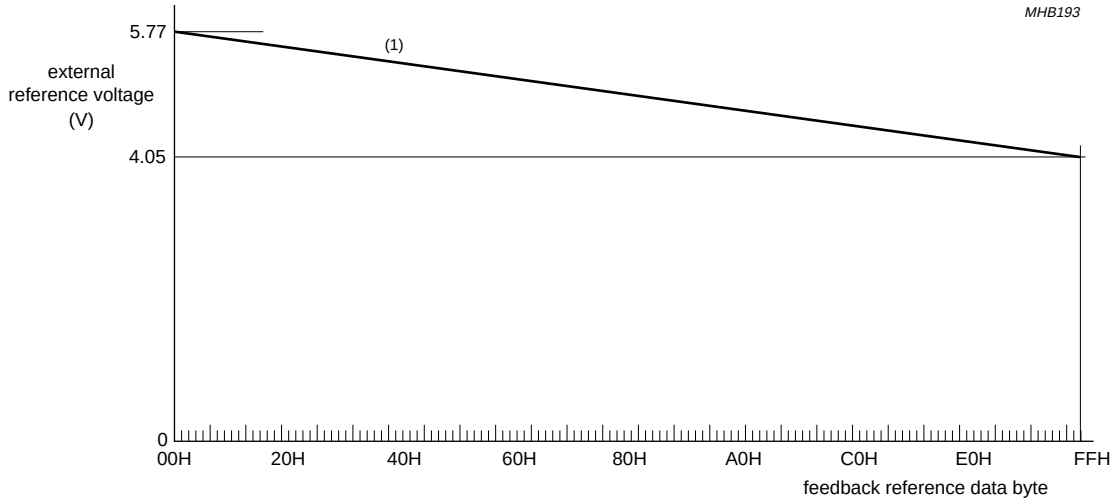


Fig.11 Gain control characteristic.



(1) Control bit FPOL = 0.
(2) Control bits FPOL = 1, BLH2 = 1, BLH1 = 1.
(3) Control bits FPOL = 1, BLH2 = 1, BLH1 = 0.
(4) Control bits FPOL = 1, BLH2 = 0, BLH1 = 1.
(5) Control bits FPOL = 1, BLH2 = 0, BLH1 = 0.

Fig.12 Internal feedback reference voltages.



(1) Control bit FPOL = 1.

Fig.13 External feedback reference voltages.

11 I²C-BUS PROTOCOL

Table 1 Slave address

A6(1)	**A5**(1)	**A4**(1)	**A3**(1)	**A2**(1)	**A1**(1)	**A0**(1)	$\overline{\mathbf{W}}$(2)
1	0	0	0	1	0	0	0

Notes

1. Address bit.
2. Write bit.

Table 2 Slave receiver format

S(1)	SLAVE ADDRESS A(2)	SUBADDRESS A(3)	DATA BYTE A(4)	P(5)

Notes

1. START condition.
2. A = acknowledge.
3. All subaddresses within the range 00H to 09H are automatically incremented. The subaddress counter wraps around from 09H to 00H. For subaddresses within the range 80H to 8FH no auto-increment takes place. Subaddresses outside the ranges 00H to 0FH and 80H to 8FH are acknowledged by the device but neither auto-increment nor any other internal operation takes place.
4. Single data byte in case of no auto-increment of subaddresses. More than one data byte with auto-increment of subaddresses.
5. STOP condition.

Table 3 Subaddress byte format

FUNCTION	SUBADDRESS(1)		SUBADDRESS BYTE							
	DIRECT MODE	BUFFERED MODE	S7(2)	S6(2)	S5(2)	S4(2)	S3(2)	S2(2)	S1(2)	S0(2)
Control register	00H	80H	B(3)	0	0	0	0	0	0	0
Brightness control	01H	81H	B(3)	0	0	0	0	0	0	1
Contrast control	02H	82H	B(3)	0	0	0	0	0	1	0
OSD contrast control	03H	83H	B(3)	0	0	0	0	0	1	1
Gain control channel 1	04H	84H	B(3)	0	0	0	0	1	0	0
Gain control channel 2	05H	85H	B(3)	0	0	0	0	1	0	1
Gain control channel 3	06H	86H	B(3)	0	0	0	0	1	1	0
Black level reference channel 1	07H	87H	B(3)	0	0	0	0	1	1	1
Black level reference channel 2	08H	88H	B(3)	0	0	0	1	0	0	0
Black level reference channel 3	09H	89H	B(3)	0	0	0	1	0	0	1
	0AH to 0FH	8AH to 8FH	not used							

Notes

1. The most significant bit (MSB) of the subaddress enables an I²C-bus transmission in direct or in buffered mode (see note 3). Subaddresses outside the ranges 00H to 0FH and 80H to 8FH are not used.
2. Subaddress bit.
3. Most significant bit of subaddress byte. I²C-bus transmission in **direct mode: B = 0**. I²C-bus transmission in **buffered mode: B = 1**.

Table 4 Subaddress and data byte format

FUNCTION	SUBADDRESS(1)		DATA BYTE(2)								NOMINAL VALUE(3)
	DIRECT MODE	BUFFERED MODE	D7(4)	D6(4)	D5(4)	D4(4)	D3(4)	D2(4)	D1(4)	D0(4)	
Control register	00H	80H	X(5)	X(5)	BLH2	BLH1	FPOL	DISV	DISO	PEDST	08H
Brightness control	01H	81H	X(5)	X(5)	A15	A14	A13	A12	A11	A10	10H
Contrast control	02H	82H	X(5)	X(5)	A25	A24	A23	A22	A21	A20	26H
OSD contrast control	03H	83H	X(5)	X(5)	X(5)	X(5)	A33	A32	A31	A30	0FH
Gain control channel 1	04H	84H	X(5)	X(5)	A45	A44	A43	A42	A41	A40	3FH
Gain control channel 2	05H	85H	X(5)	X(5)	A55	A54	A53	A52	A51	A50	3FH
Gain control channel 3	06H	86H	X(5)	X(5)	A65	A64	A63	A62	A61	A60	3FH
Black level reference channel 1	07H	87H	A77	A76	A75	A74	A73	A72	A71	A70	–
Black level reference channel 2	08H	88H	A87	A86	A85	A84	A83	A82	A81	A80	–
Black level reference channel 3	09H	89H	A97	A96	A95	A94	A93	A92	A91	A90	–

Notes

1. See Table 3 (Subaddress byte format).
2. The least significant bit (LSB) of an analog alignment register is defined as AX0 (data bit D0).
3. Under certain conditions the nominal values lead to nominal colour signals etc. (see note 3 of Chapter “Characteristics”).

   After power-up and after internal power-on reset of the I²C-bus the registers are set to the following values:

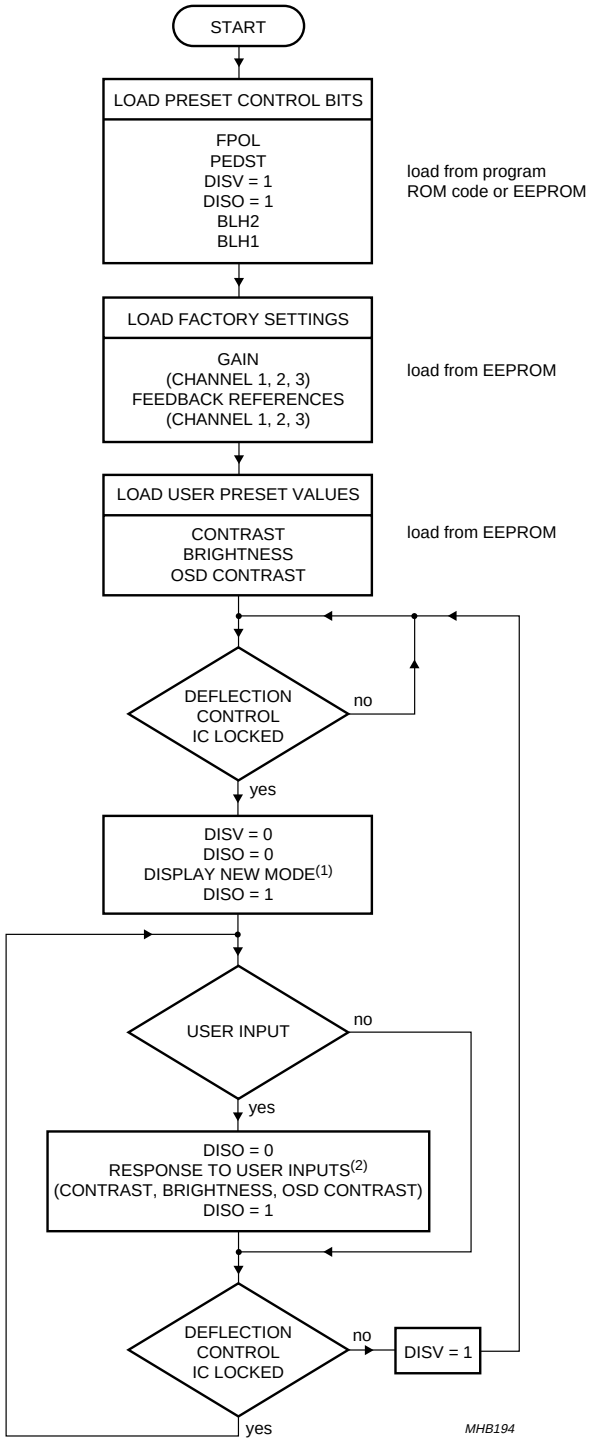
   a) Control bit FPOL to logic 1.

   b) Control bits BLH2, BLH1, DISV, DISO and PEDST to logic 0.

   c) All other alignment registers to logic 0 (minimum value for control registers).
4. Data bit.
5. X means don’t care but for software compatibility with other video ICs with the same slave address, they are preferably set to logic 0.

Table 5 Control register

BIT		FUNCTION
PEDST = 0		no pedestal blanking
PEDST = 1		pedestal blanking enabled
DISO = 0		OSD signals enabled
DISO = 1		OSD signals disabled
DISV = 0		video signals enabled
DISV = 1		video signals disabled
FPOL = 0		negative feedback polarity; pins 23, 20 and 17 as external feedback inputs; no external feedback reference voltages
FPOL = 1		positive feedback polarity; pins 23, 20 and 17 as external reference voltage outputs; internal feedback of signal outputs
BLH2 = 0	BLH1 = 0	for positive feedback polarity only: internal feedback reference voltage switched to approximately 0.75 V
BLH2 = 0	BLH1 = 1	for positive feedback polarity only: internal feedback reference voltage switched to approximately 1.0 V
BLH2 = 1	BLH1 = 0	for positive feedback polarity only: internal feedback reference voltage switched to approximately 1.25 V
BLH2 = 1	BLH1 = 1	for positive feedback polarity only: internal feedback reference voltage switched to approximately 1.5 V



(1) Only synchronized video should be displayed. Each new mode can be displayed by OSD.

(2) Data transmission should be synchronized with vertical blanking of the monitor.

Fig.14 I²C-bus control flow.

12 TEST AND APPLICATION INFORMATION

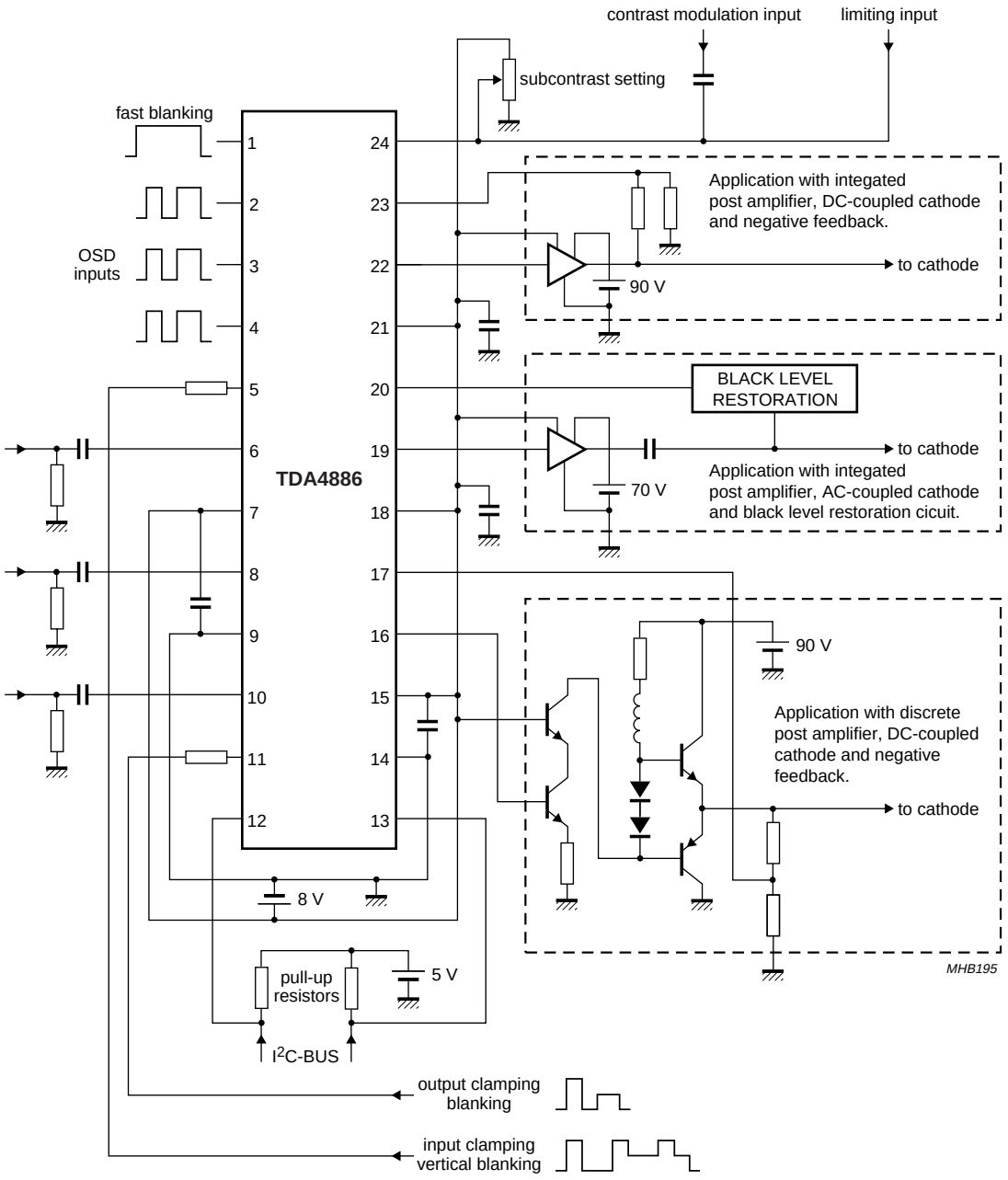


Fig.15 Basic applications for different kinds of post amplifiers with DC or AC coupling.

12.1 Test boards

For high frequency measurements a special test application and printed-circuit board with only a few external components is built. It utilizes the internal positive feedback of the output signals during output clamping with control bit FPOL = 1. Figure 16 shows the test application circuit and Figs 17 and 18 show the layout and mounting of the double-sided printed-circuit board. Most components are of SMD type. Short HF loops and minimum crosstalk between the channels and between signal inputs and outputs are achieved by properly shaped ground areas.

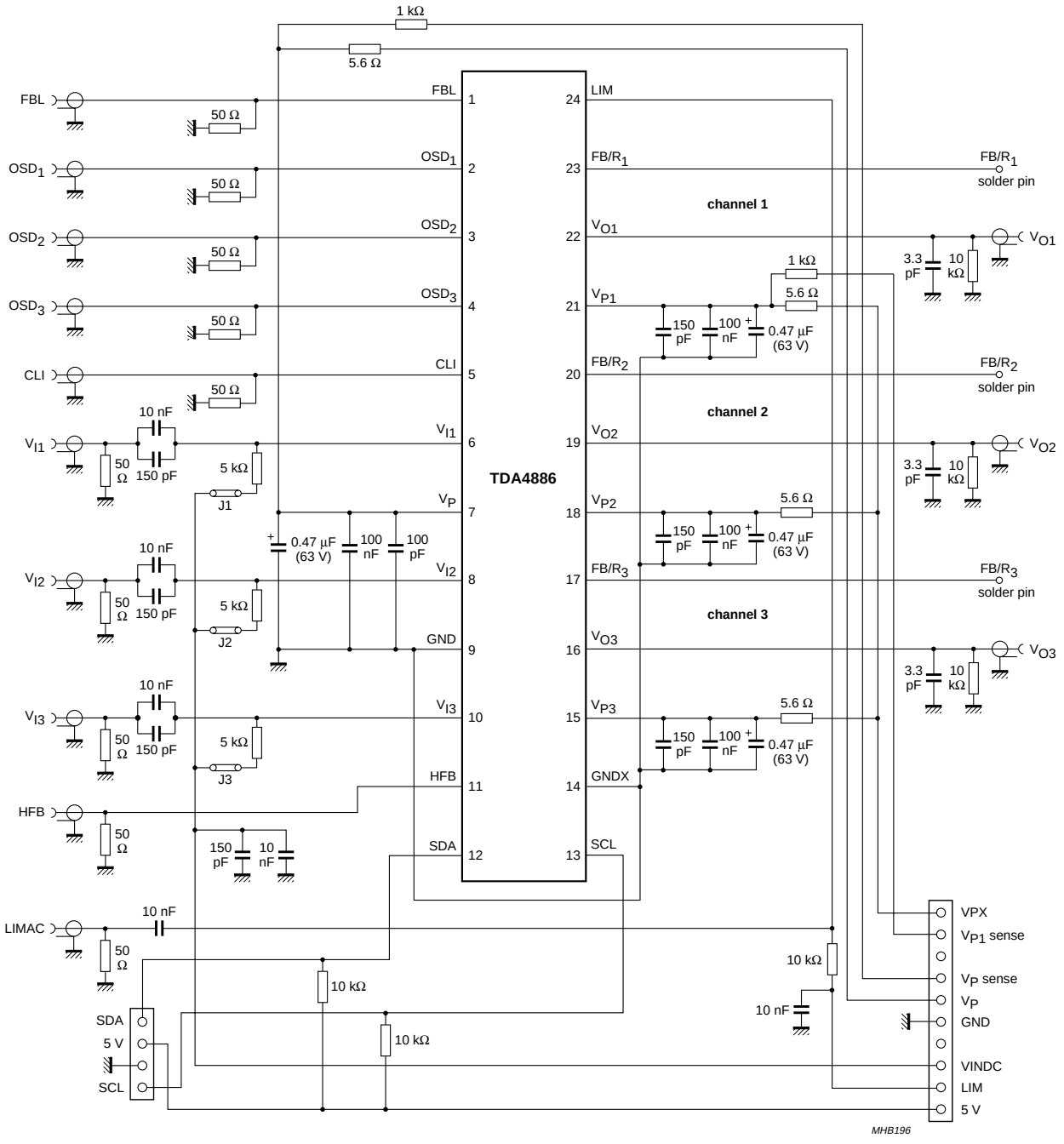
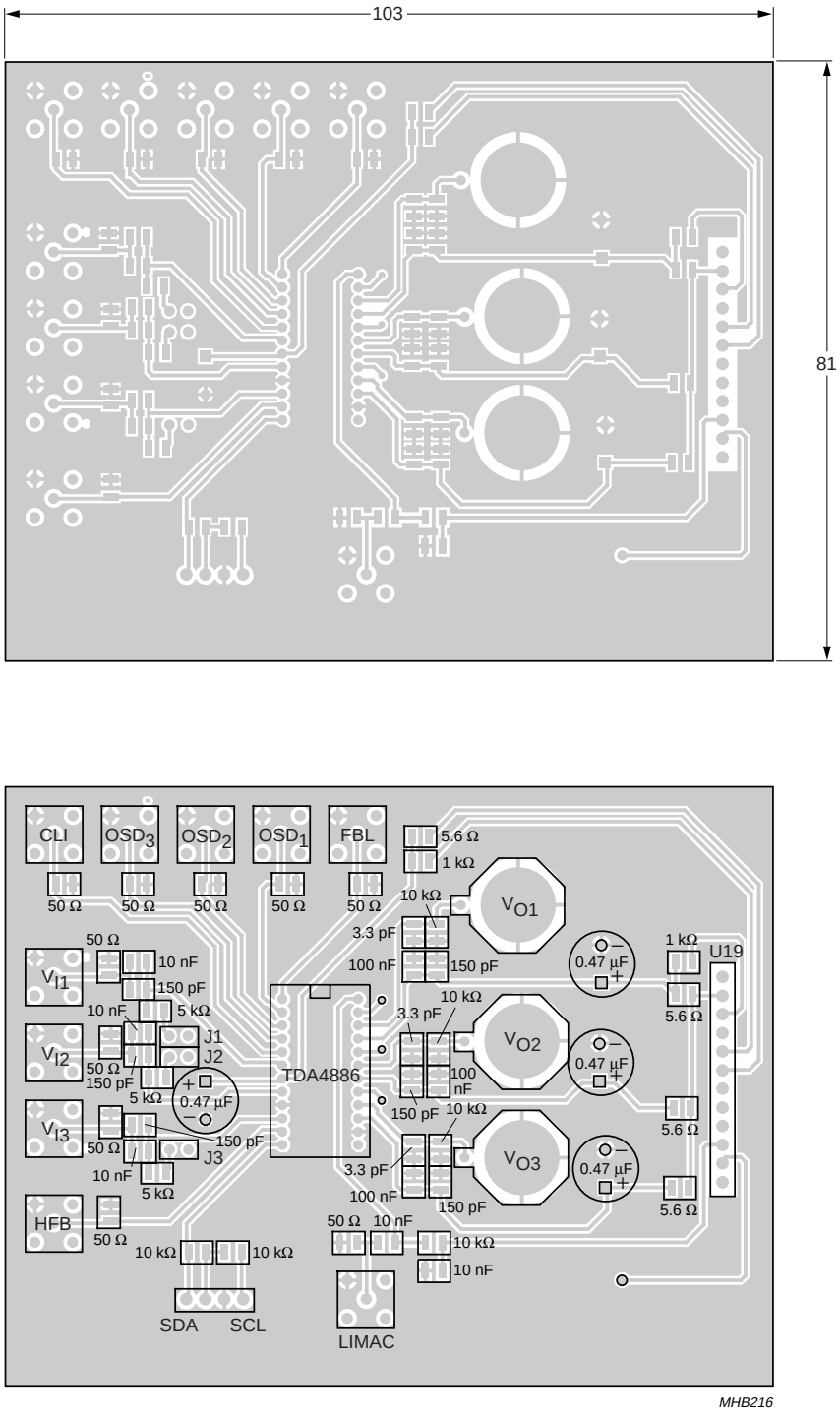
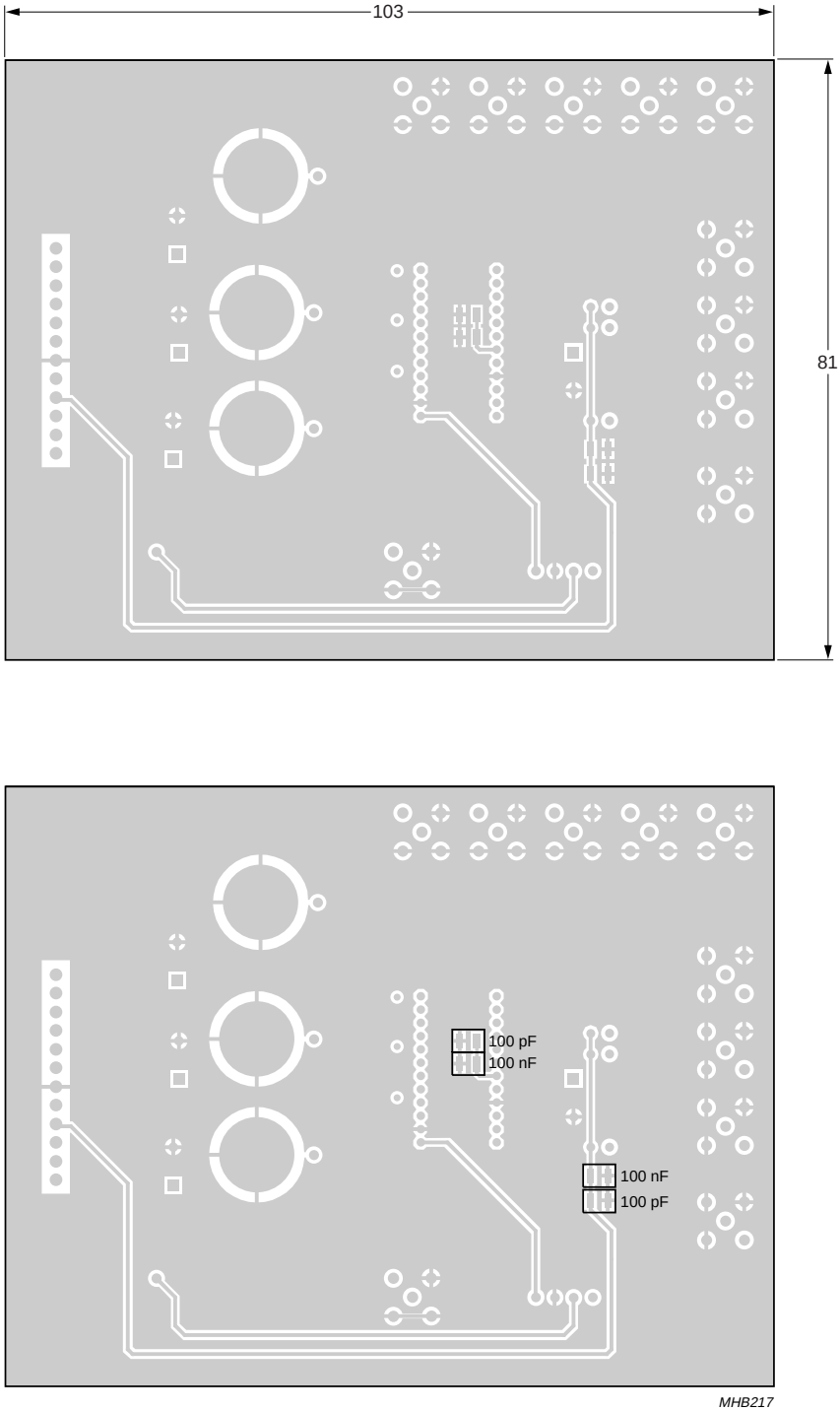


Fig.16 Test board utilizing internal positive feedback only (FPOL = 1).



Dimensions are in mm.

Fig.17 Top view of the printed-circuit board (for the bottom view see Fig.18).



Dimensions are in mm.

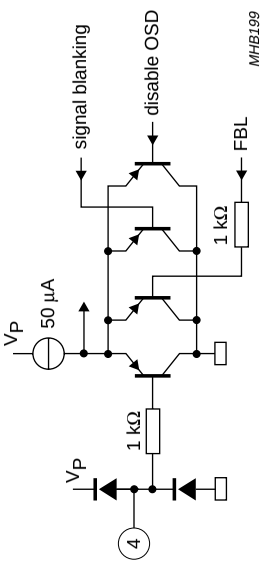
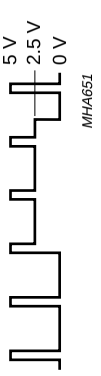
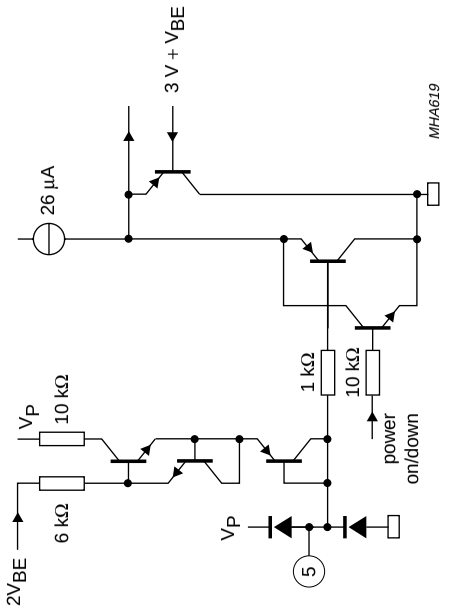
Fig.18 Bottom view of the printed-circuit board (for the top view see Fig.17).

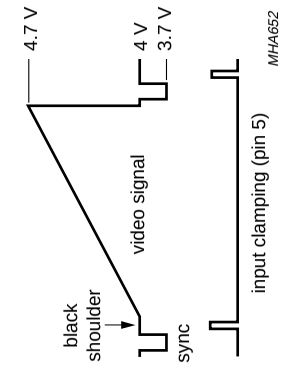
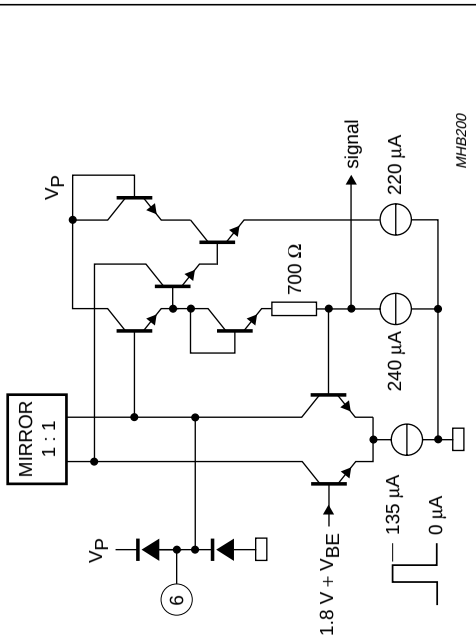
12.2 Recommendations for building the application board

- General
  - Double-sided board
  - Short HF loops by large ground plane on the rear
  - SMD components with minimum parasitics.
- Voltage outputs
  - Capacitive loads as small as possible
  - Be aware of internal output resistance (typically 75 Ω).
- Supply voltages
  - Capacitors as near as possible to the pins
  - Use electrolytic capacitors with small serial resistance and inductance.

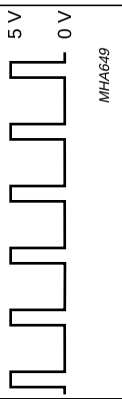
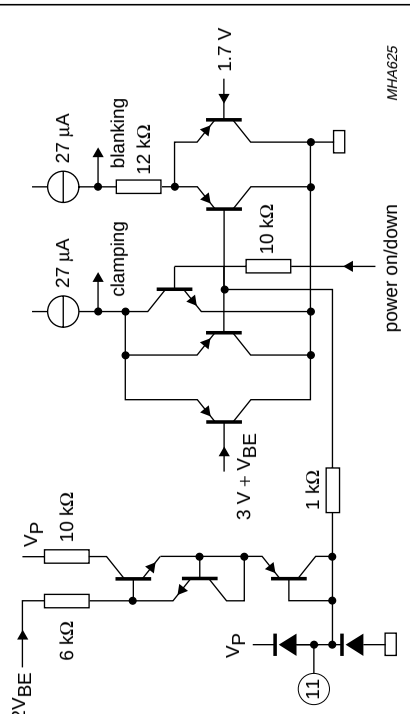
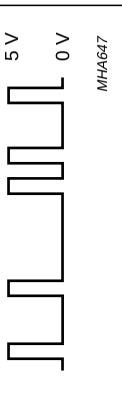
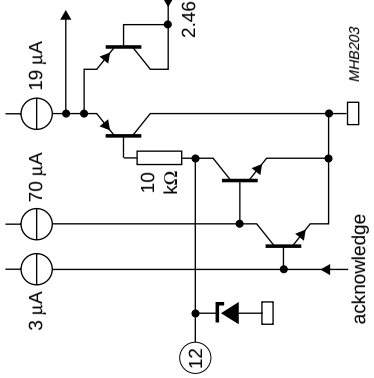
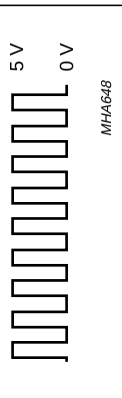
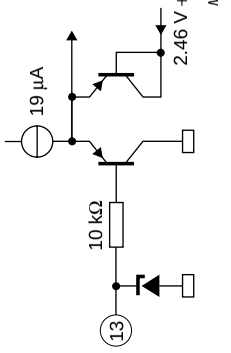
13 INTERNAL CIRCUITRY

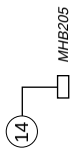
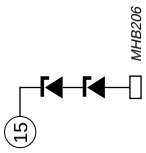
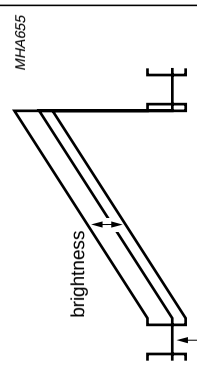
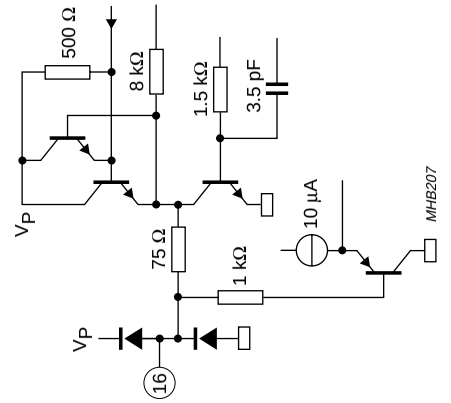
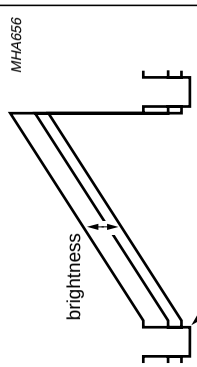
PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
1	FBL; fast blanking input for OSD insertion	open-circuit base		
2	OSD_1; OSD input channel 1	open-circuit base		
3	OSD_2; OSD input channel 2	open-circuit base		

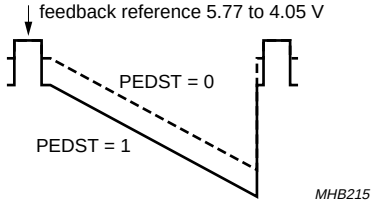
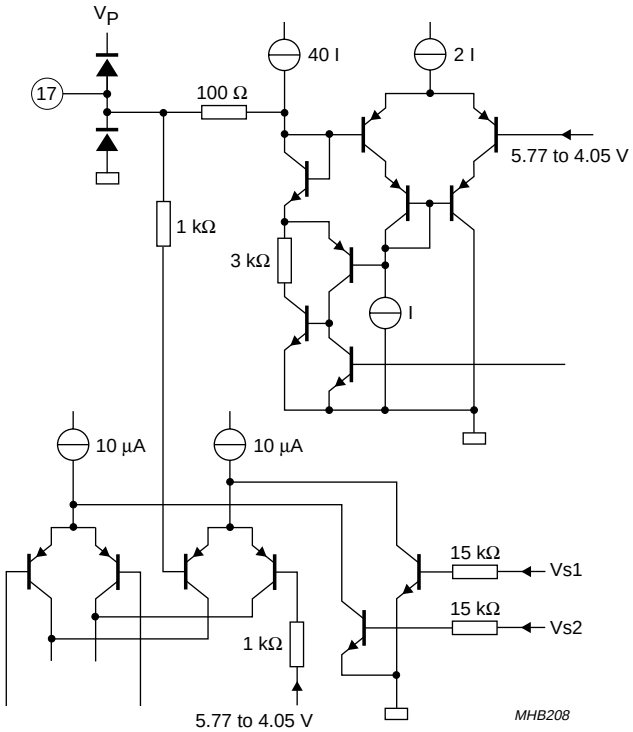
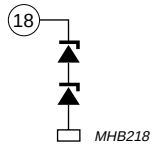
PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
4	OSD_3; OSD input channel 3	open-circuit base		
5	CLI; vertical blanking input (input clamping)	V_5 > 0.2 V: open-circuit base		
		$V_5 \leq$ 0.2 V: source current rising with decreasing voltage		

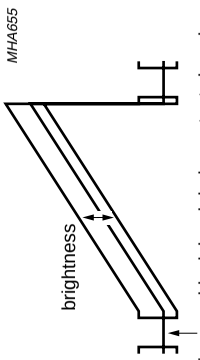
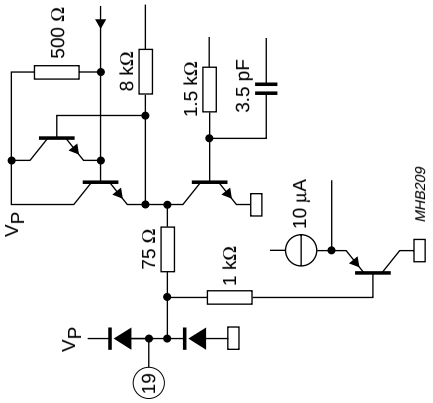
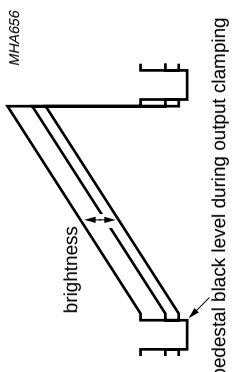
PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
6	V_{I1}; signal input channel 1	outside clamping pulse: open-circuit base with base current compensation		
	during clamping: −135 to +135 µA			
7	V_P; supply voltage	21 mA		

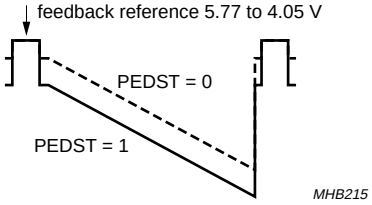
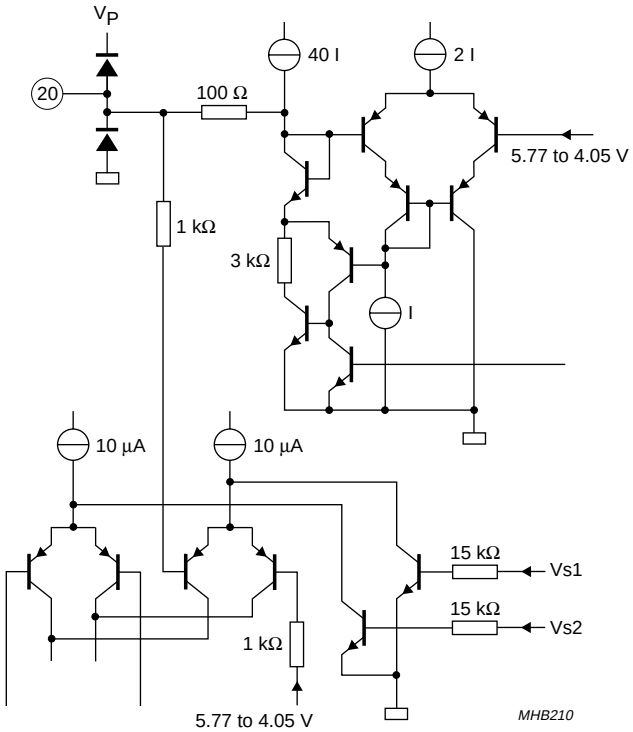
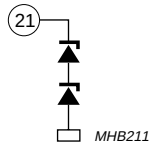
PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
8	V_{I2}; signal input channel 2	outside clamping pulse: open-circuit base with base current compensation during clamping: −135 to +135 μA		
9	GND; ground			
10	V_{I3}; signal input channel 3	outside clamping pulse: open-circuit base with base current compensation during clamping: −135 to +135 μA		

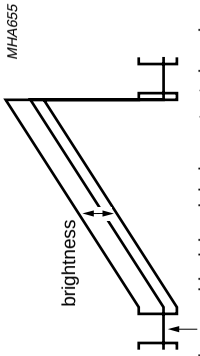
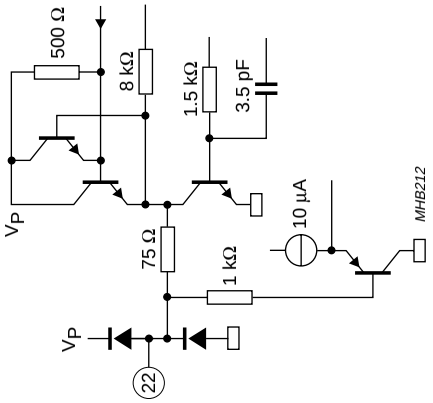
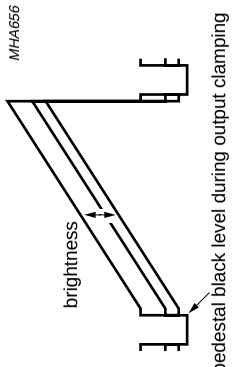
PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
11	HFB; horizontal flyback input (output clamping, blanking)	V_{11} > 0.2 V: open-circuit base V_{11} ≤ 0.2 V: source current rising with decreasing voltage		
12	SDA; I²C-bus serial data input/output	no acknowledge: open-circuit base during acknowledge: I_{12} = 4 mA		
13	SCL; I²C-bus clock input	open-circuit base		

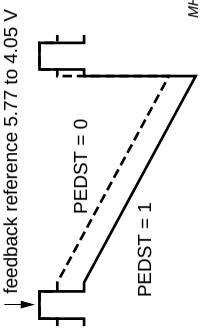
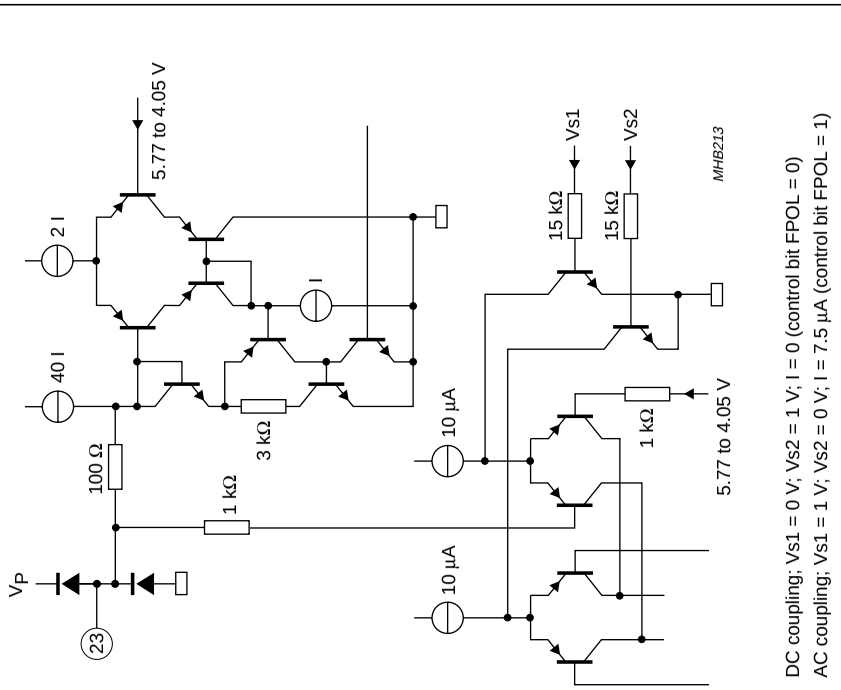
PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
14	GNDX; signal channel ground			
15	V_{P3}; supply voltage channel 3	I_{15} = 21 mA		
16	V_{O3}; signal output channel 3	reference black level 0.1 to 2.8 V	 control bit PEDST = 0	
		pedestal black level 0.1 to 2.8 V	 control bit PEDST = 1	

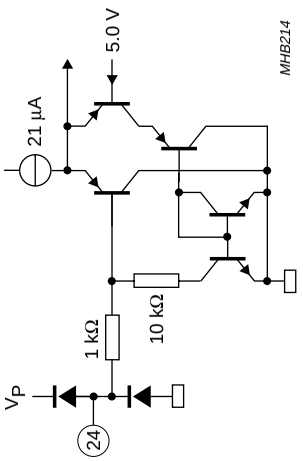
PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
17	FB/R_3; feedback input/ reference voltage output channel 3	open-circuit base	 control bit FPOL = 0	 DC coupling; Vs1 = 0 V; Vs2 = 1 V; I = 0 (control bit FPOL = 0) AC coupling; Vs1 = 1 V; Vs2 = 0 V; I = 7.5 µA (control bit FPOL = 1)
		–300 to +300 µA; 5.77 to 4.05 V	control bit FPOL = 1	
18	V_{P2}; supply voltage channel 2	I_{18} = 21 mA		

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
19	V_{O2}; signal output channel 2	reference black level 0.1 to 2.8 V	 control bit PEDST = 0	
		pedestal black level 0.1 to 2.8 V	 control bit PEDST = 1	

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
20	FB/R_2; feedback input/ reference voltage output channel 2	open-circuit base	 control bit FPOL = 0	 DC coupling; Vs1 = 0 V; Vs2 = 1 V; I = 0 (control bit FPOL = 0) AC coupling; Vs1 = 1 V; Vs2 = 0 V; I = 7.5 µA (control bit FPOL = 1)
		–300 to +300 µA; 5.77 to 4.05 V	control bit FPOL = 1	
21	V_{P1}; supply voltage channel 1	I_{21} = 21 mA		

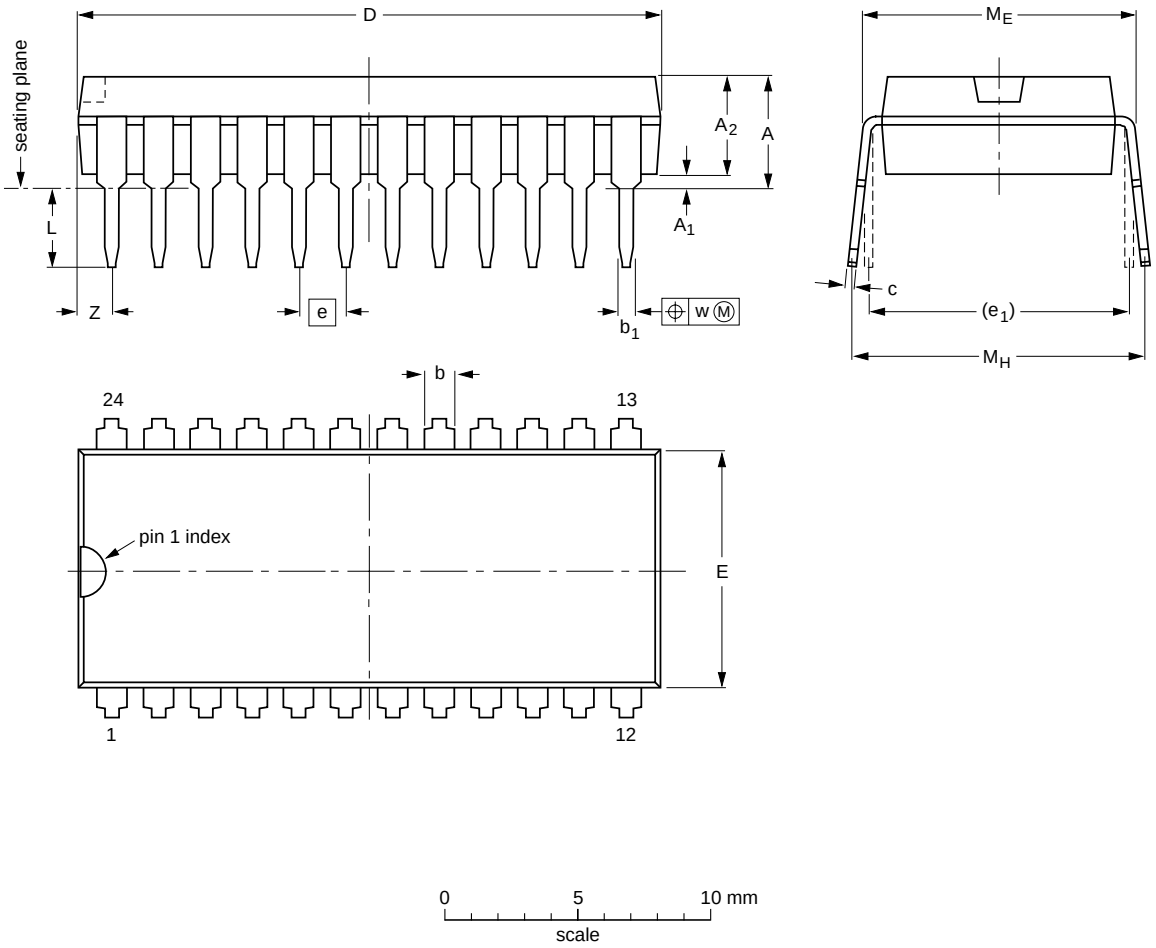
PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
22	V_{O1}; signal output channel 1	reference black level 0.1 to 2.8 V	 control bit PEDST = 0	
		pedestal black level 0.1 to 2.8 V	 control bit PEDST = 1	

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
23	FB/R_1; feedback input/ reference voltage output channel 1	open-circuit base		
		control bit FPOL = 0		
		–300 to +300 µA; 5.77 to 4.05 V	control bit FPOL = 1	

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC		WAVEFORM	EQUIVALENT CIRCUIT
24	LIM; beam current limiting input	open-circuit voltage V_{24} = 5.0 V	V_{24} < 4.5 V: open-circuit base		

14 PACKAGE OUTLINE

SDIP24: plastic shrink dual in-line package; 24 leads (400 mil) **SOT234-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	22.3 21.4	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT234-1						~~92-11-17~~ 95-02-04

15 SOLDERING

15.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

15.2 Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

15.3 Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

16 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

17 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

18 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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