- **Improved Stability Over Supply Voltage and Temperature Ranges**
- **Constant-Current Outputs**
- **High Speed**
- **Standard Supply Voltages**
- **High Output Impedance**
- **High Common-Mode Output Voltage Range . . . –3 V to 10 V**
- **TTL-Input Compatibility**
- **Inhibitor Available for Driver Selection**
- **Glitch Free During Power Up/Power Down**
- **SN75112 and External Circuit Meets or Exceeds the Requirements of CCITT Recommendation V.35**

SN55110A . . . J OR W PACKAGE
SN75110A . . . D, N, OR NS PACKAGE
SN75112 . . . D OR N PACKAGE
(TOP VIEW)

1A	1	14	V_{CC+}
1B	2	13	1Y
1C	3	12	1Z
2C	4	11	V_{CC-}
2A	5	10	D
2B	6	9	2Z
GND	7	8	2Y
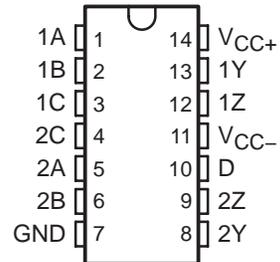
SN55110A . . . FK PACKAGE
(TOP VIEW)
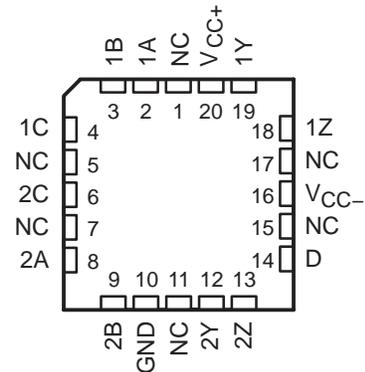
NC – No internal connection

## description/ordering information

The SN55110A, SN75110A, and SN75112 dual line drivers have improved output current regulation with supply-voltage and temperature variations. In addition, the higher current of the SN75112 (27 mA) allows data to be transmitted over longer lines. These drivers offer optimum performance when used with the SN55107A, SN75107A, and SN75108A line receivers.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 25	SN75110AN	SN75110AN
			SN75112N	SN75112N
	SOIC (D)	Tube of 50	SN75110AD	SN75110A
		Reel of 2500	SN75110ADR	
		Tube of 50	SN75112D	SN75112
		Reel of 2500	SN75112DR	
	SOP (NS)	Reel of 2000	SN75110ANSR	SN75110A
–55°C to 125°C	CDIP (J)	Tube of 25	SN55110AJ	SN55110AJ
			SNJ55110AJ	SNJ55110AJ
	CFP (W)	Tube of 150	SNJ55110AW	SNJ55110AW
	LCCC (FK)	Tube of 55	SNJ55110AFK	SNJ55110AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

description/ordering information (continued)

These drivers feature independent channels with common voltage supply and ground terminals. The significant difference between the three drivers is in the output-current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by low logic levels on the enable inputs. The output current nominally is 12 mA for the '110A devices and is 27 mA for the SN75112.

The enable/inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor (enable D), common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high. The output impedance of a transistor is biased to cutoff.

The driver outputs have a common-mode voltage range of –3 V to 10 V, allowing common-mode voltage on the line without affecting driver performance.

All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at 2 V for high-logic-level input conditions and 0.8 V for low-logic-level input conditions. These tests ensure 400-mV noise margin when interfaced with TTL Series 54/74 devices.

The SN55110A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN75110A and SN75112 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

LOGIC INPUTS		ENABLE INPUTS		OUTPUTS[†]	
A	**B**	**C**	**D**	**Y**	**Z**
X	X	L	X	Off	Off
X	X	X	L	Off	Off
L	X	H	H	On	Off
X	L	H	H	On	Off
H	H	H	H	Off	On

H = high level, L = low level, X = irrelevant
[†] When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

schematic (each driver)
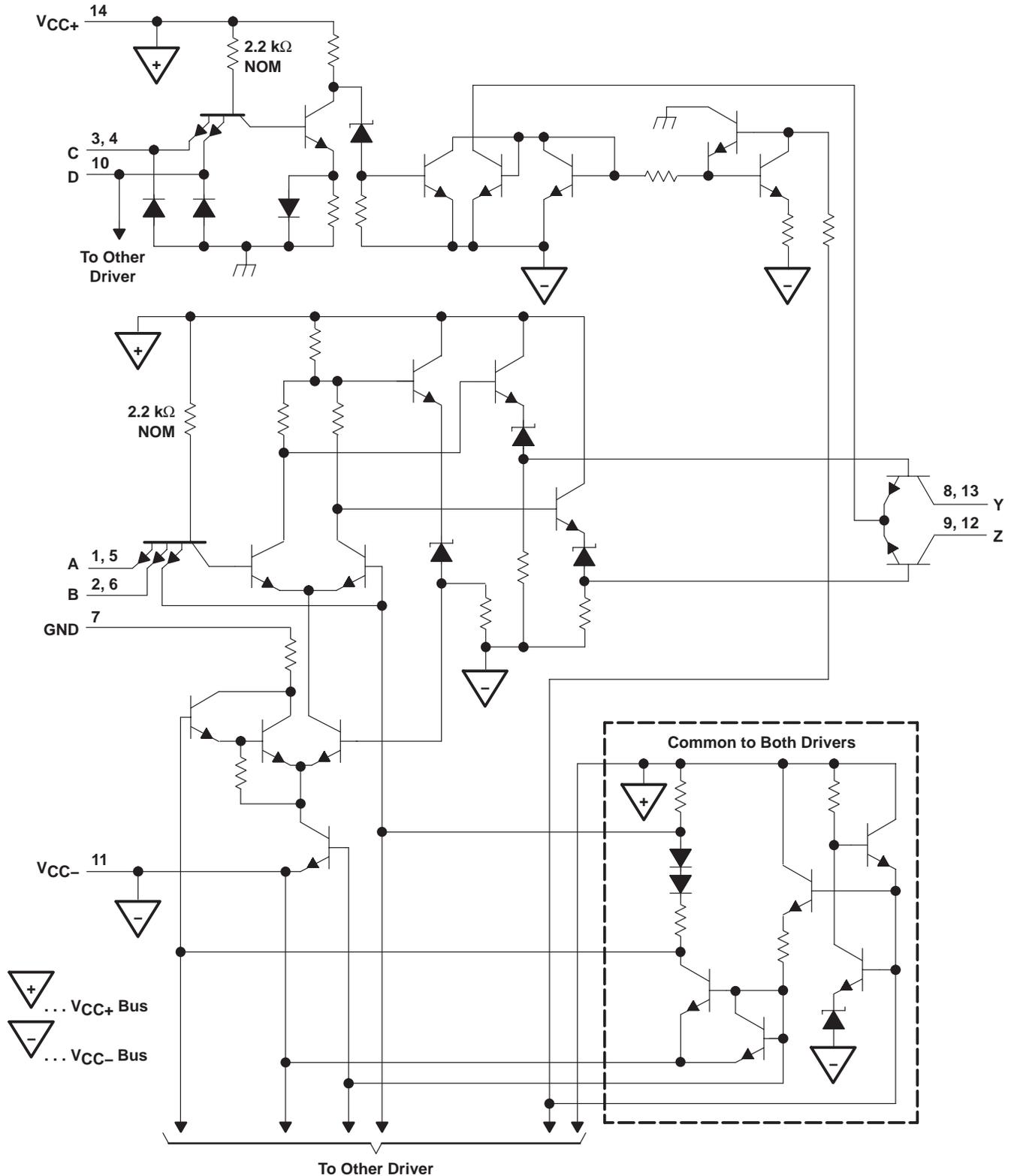
Pin numbers shown are for the D, J, N, NS, and W packages.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage: V_{CC+} (see Note 1)	7 V
V_{CC-} (see Note 1)	−7 V
Input voltage, V_I	5.5 V
Output voltage range, V_O	−5 V to 12 V

Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package . . . . 86°C/W
N package . . . . 80°C/W
NS package . . . . 76°C/W
Package thermal impedance, θ_{JC} (see Notes 4 and 5): FK package . . . . 13.42°C/W
J package . . . . 15.05°C/W
W package . . . . 14.65°C/W
Operating virtual junction temperature . . . . 150°C
Case temperature for 60 seconds: FK package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package . . . . 300°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. Maximum power dissipation is a function of T_J(max), θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(max) - T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
5. The package thermal impedance is calculated in accordance with MIL-STD-883.

recommended operating conditions (see Note 6)

		SN55110A			SN75110A SN75112			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC+}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{CC-}	Supply voltage	−4.5	−5	−5.5	−4.75	−5	−5.25	V
	Positive common-mode output voltage	0		10	0		10	V
	Negative common-mode output voltage	0		−3	0		−3	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level output voltage			0.8			0.8	V
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 6: When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN55110A SN75110A			SN75112			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	$V_{CC\pm}$ = MIN, I_L = –12 mA		–0.9	–1.5		–0.9	–1.5	V
$I_{O(on)}$	On-state output current	$V_{CC\pm}$ = MAX, V_O = 10 V		12	15		27	40	mA
		V_{CC} = MIN to MAX, V_O = –1 V to 1 V, T_A = 25°C				24	28	32	
		$V_{CC\pm}$ = MIN, V_O = –3 V	6.5	12		15	27		
$I_{O(off)}$	Off-state output current	$V_{CC\pm}$ = MIN, V_O = 10 V			100			100	µA
I_I	Input current at maximum input voltage	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 5.5 V			1			1	mA
		D input				2			2	
I_{IH}	High-level input current	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 2.4 V			40			40	µA
		D input				80			80	
I_{IL}	Low-level input current	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 0.4 V			–3			–3	mA
		D input				–6			–6	
$I_{CC+(on)}$	Supply current from V_{CC} with driver enabled	$V_{CC\pm}$ = MAX, A and B inputs at 0.4 V, C and D inputs at 2 V		23	35		25	40	mA
$I_{CC–(on)}$	Supply current from $V_{CC–}$ with driver enabled	$V_{CC\pm}$ = MAX, A and B inputs at 0.4 V, C and D inputs at 2 V		–34	–50		–65	–100	mA
$I_{CC+(off)}$	Supply current from $V_{CC–}$ with driver inhibited	$V_{CC\pm}$ = MAX, A, B, C, and D inputs at 0.4 V		21			30		mA
$I_{CC–(off)}$	Supply current from $V_{CC\pm}$ with driver inhibited	$V_{CC\pm}$ = MAX, A, B, C, and D inputs at 0.4 V		–17			–32		mA

† For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC+} = 5 V, $V_{CC–}$ = –5 V, T_A = 25°C.

switching characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C (see Figure 1)

| PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y or Z	C_L = 40 pF,	R_L = 50 Ω,		9	15	ns
t_{PHL}						9	15	
t_{PLH}	C or D	Y or Z	C_L = 40 pF,	R_L = 50 Ω,		16	25	ns
t_{PHL}						13	25	

§ t_{PLH} = propagation delay time, low- to high-level output
t_{PHL} = propagation delay time, high- to low-level output

TEXAS INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION
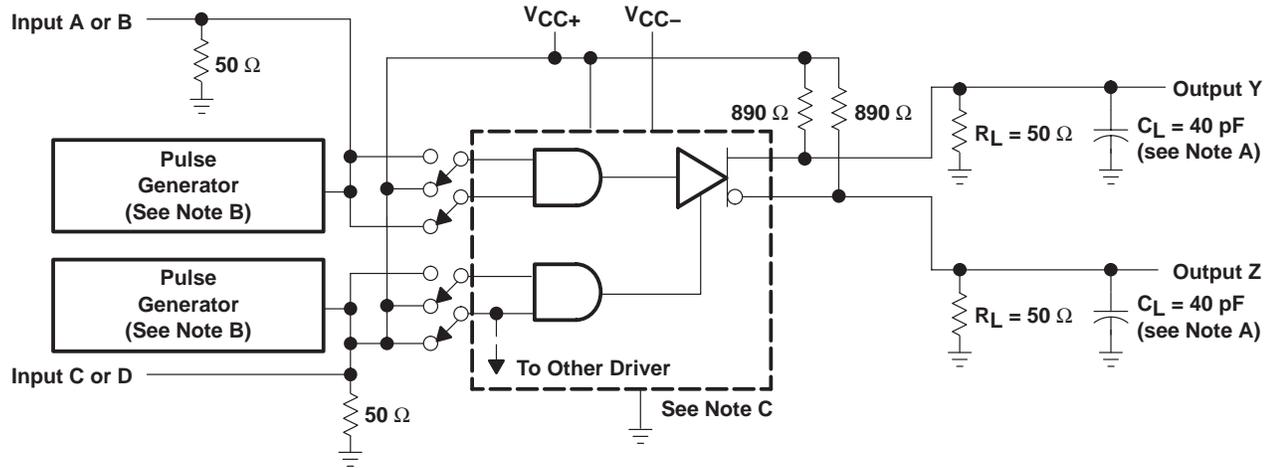
TEST CIRCUIT
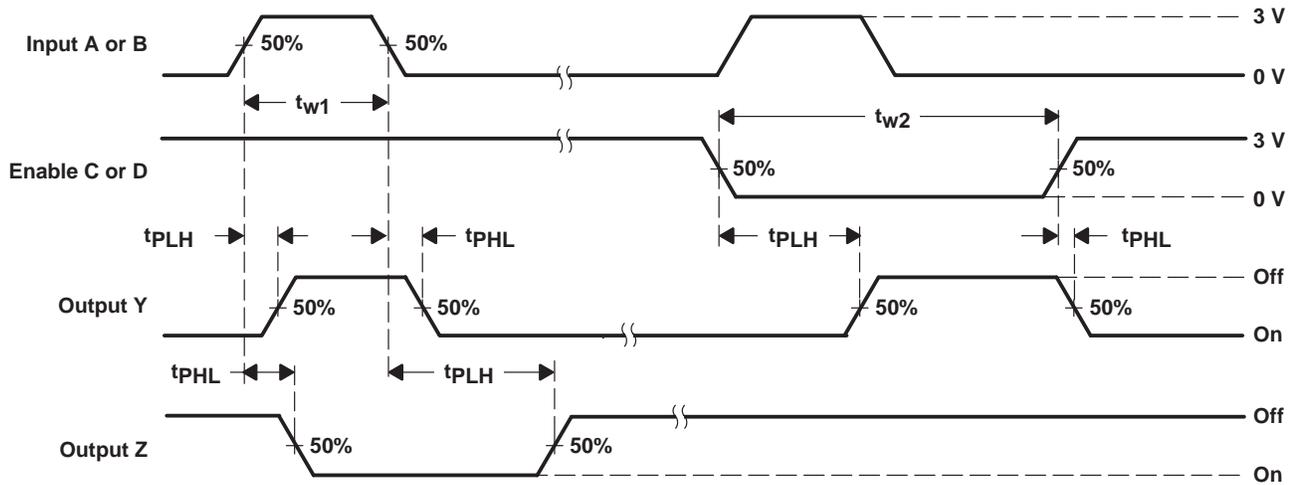
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generators have the following characteristics: Z_O = 50 Ω, t_r = t_f = 10 ± 5 ns, t_{w1} = 500 ns, PRR ≤ 1 MHz, t_{w2} = 1 μs, PRR ≤ 500 kHz.
C. For simplicity, only one channel and the enable connections are shown.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SN55110A, SN75110A
ON-STATE OUTPUT CURRENT
vs
NEGATIVE SUPPLY VOLTAGE

V_{CC+} = 4.5 V
V_O = −3 V
T_A = 25°C

$I_{O(on)}$ − On-State Output Current − mA

$V_{CC−}$ − Negative Supply Voltage − V
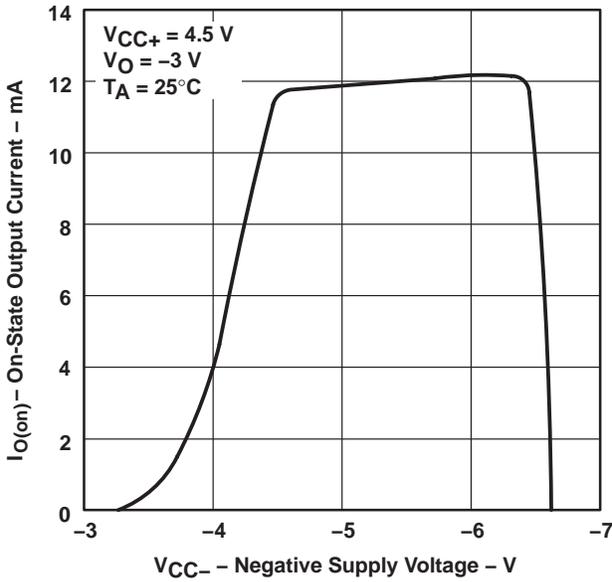
Figure 2

SN75112
ON-STATE OUTPUT CURRENT
vs
NEGATIVE SUPPLY VOLTAGE

V_{CC+} = 4.5 V
V_O = −3 V
T_A = 25°C

$I_{O(on)}$ − On-State Output Current − mA

$V_{CC−}$ − Negative Supply Voltage − V
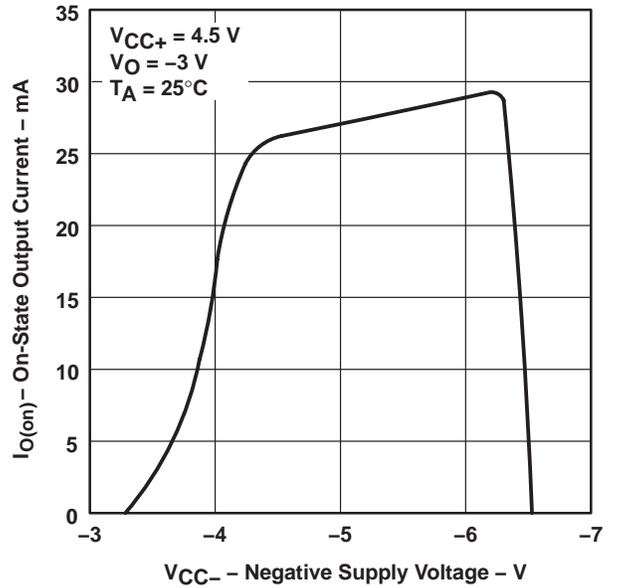
Figure 3

APPLICATION INFORMATION

special pulse-control circuit

Figure 4 shows a circuit that can be used as a pulse-generator output or in many other testing applications.

INPUT A	OUTPUTS	
	Y	Z
High	Off	On
Low	On	Off

Figure 4. Pulse-Control Circuit

APPLICATION INFORMATION

using the SN75112 as a CCITT-recommended V.35 line driver

The SN75112 dual line driver, the SN75107A dual line receiver, and some external resistors can be used to implement the data-interchange circuit of CCITT recommendation V.35 (1976) modem specification. The circuit of one channel is shown in Figure 5 and meets the requirement of the interface as specified by Appendix 11 of CCITT V.35 and is summarized in Table 1 (V.35 has been replaced by ITU V.11).

Table 1. CCITT V.35 Electrical Requirements

GENERATOR	MIN	MAX	UNIT
Source impedance, Z_{source}	50	150	Ω
Resistance to ground, R	135	165	Ω
Differential output voltage, V_{OD}	440	660	mV
10% to 90% rise time, t_r	40		ns
or		$0.01 \times ui$†	
Common-mode output voltage, V_{OC}	−0.6	0.6	V
LOAD (RECEIVER)	**MIN**	**MAX**	**UNIT**
Input impedance, Z_I	90	110	Ω
Resistance to ground, R	135	165	Ω

† ui = unit interval or minimum signal-element pulse duration
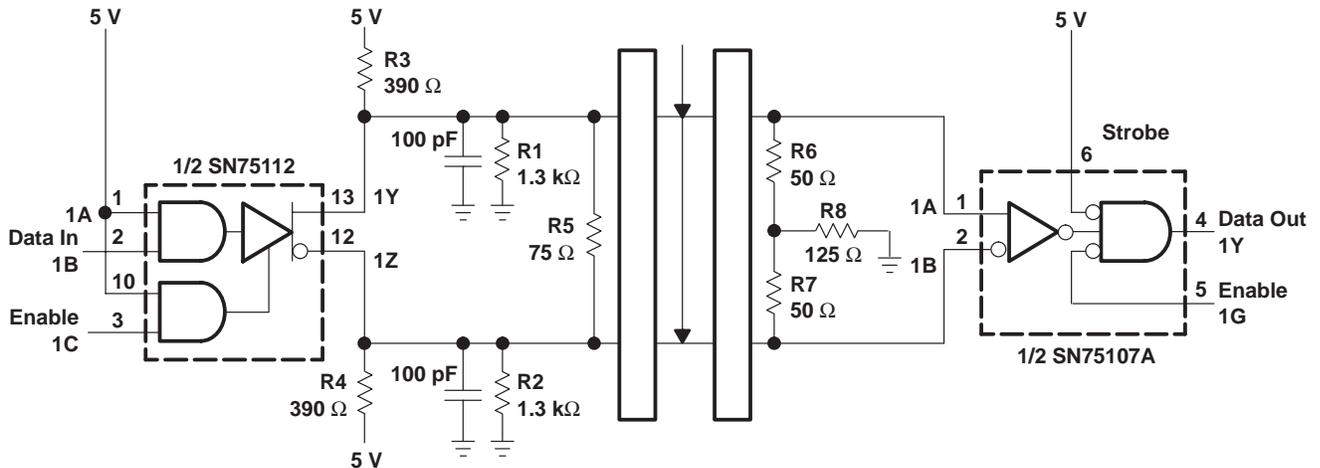
All resistors are 5%, 1/4 W.

Figure 5. CCITT-Recommended V.35 Interface Using the SN75112 and SN75107A

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-87547012A	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
5962-8754701CA	ACTIVE	CDIP	J	14	1	None	A42 SNPB	Level-NC-NC-NC
5962-8754701DA	ACTIVE	CFP	W	14	1	None	A42 SNPB	Level-NC-NC-NC
SN55110AJ	ACTIVE	CDIP	J	14	1	None	A42 SNPB	Level-NC-NC-NC
SN75110AD	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75110ADR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75110AJ	OBSOLETE	CDIP	J	14		None	Call TI	Call TI
SN75110AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75110ANSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75112D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75112DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75112N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SNJ55110AFK	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
SNJ55110AJ	ACTIVE	CDIP	J	14	1	None	A42 SNPB	Level-NC-NC-NC
SNJ55110AW	ACTIVE	CFP	W	14	1	None	A42 SNPB	Level-NC-NC-NC

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
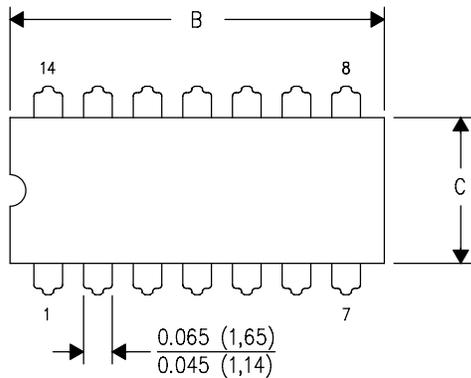
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

0.065 (1,65)
0.045 (1,14)

C

1   7

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

W (R−GDFP−F14)   CERAMIC DUAL FLATPACK

Base and Seating Plane

$\dfrac{0.045\ (1,14)}{0.026\ (0,66)}$

$\dfrac{0.260\ (6,60)}{0.235\ (5,97)}$

$\dfrac{0.006\ (0,15)}{0.004\ (0,10)}$

$\dfrac{0.080\ (2,03)}{0.045\ (1,14)}$

0.280 (7,11) MAX

$\dfrac{0.019\ (0,48)}{0.015\ (0,38)}$

0.050 (1,27)

1   14

$\dfrac{0.390\ (9,91)}{0.335\ (8,51)}$

7   8

0.005 (0,13) MIN
4 Places

$\dfrac{0.360\ (9,14)}{0.250\ (6,35)}$ $\dfrac{0.360\ (9,14)}{0.250\ (6,35)}$
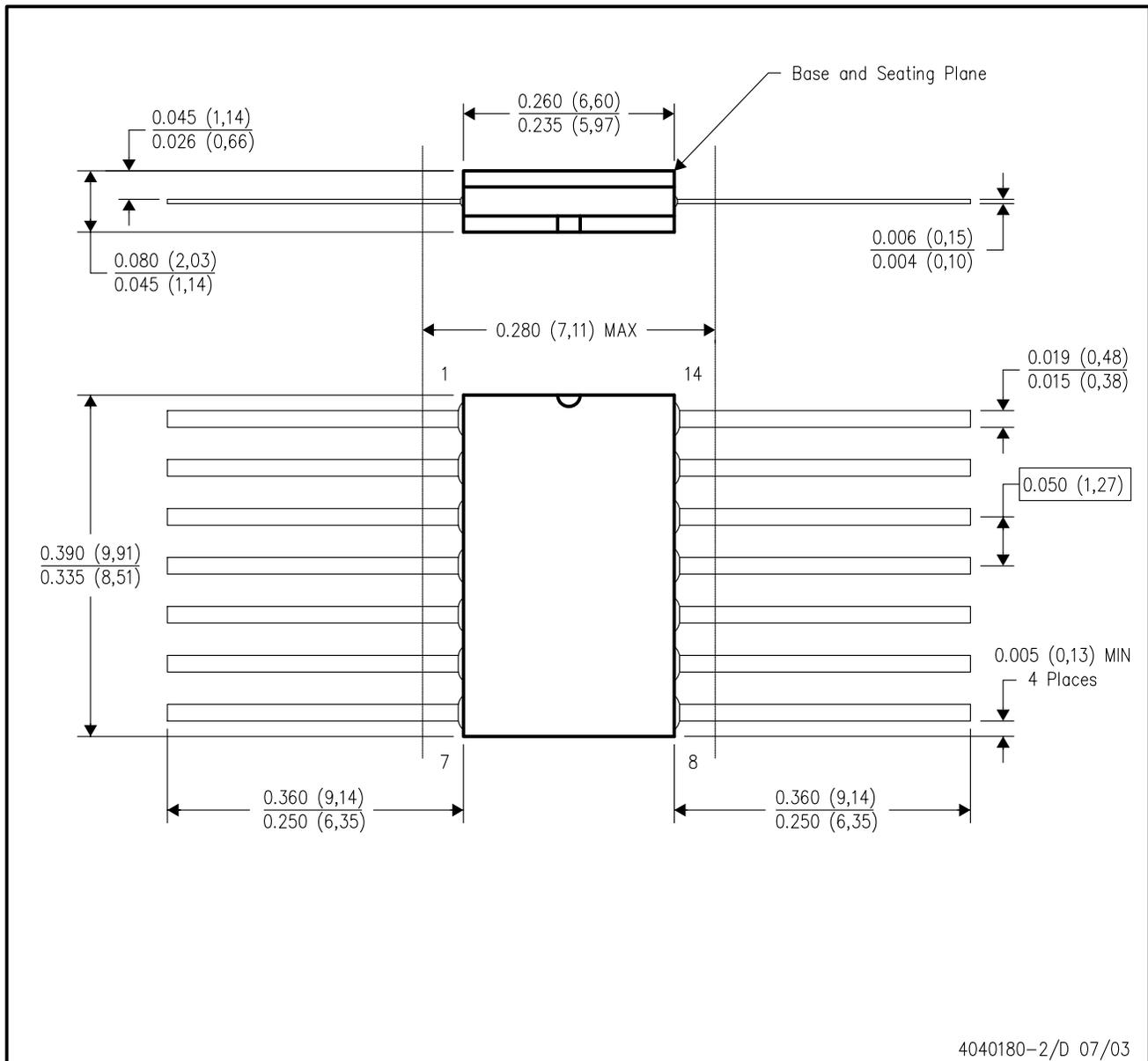
4040180−2/D 07/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package can be hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only.
         E. Falls within MIL STD 1835 GDFP1−F14 and JEDEC MO−092AB

FK (S-CQCC-N**)   **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN
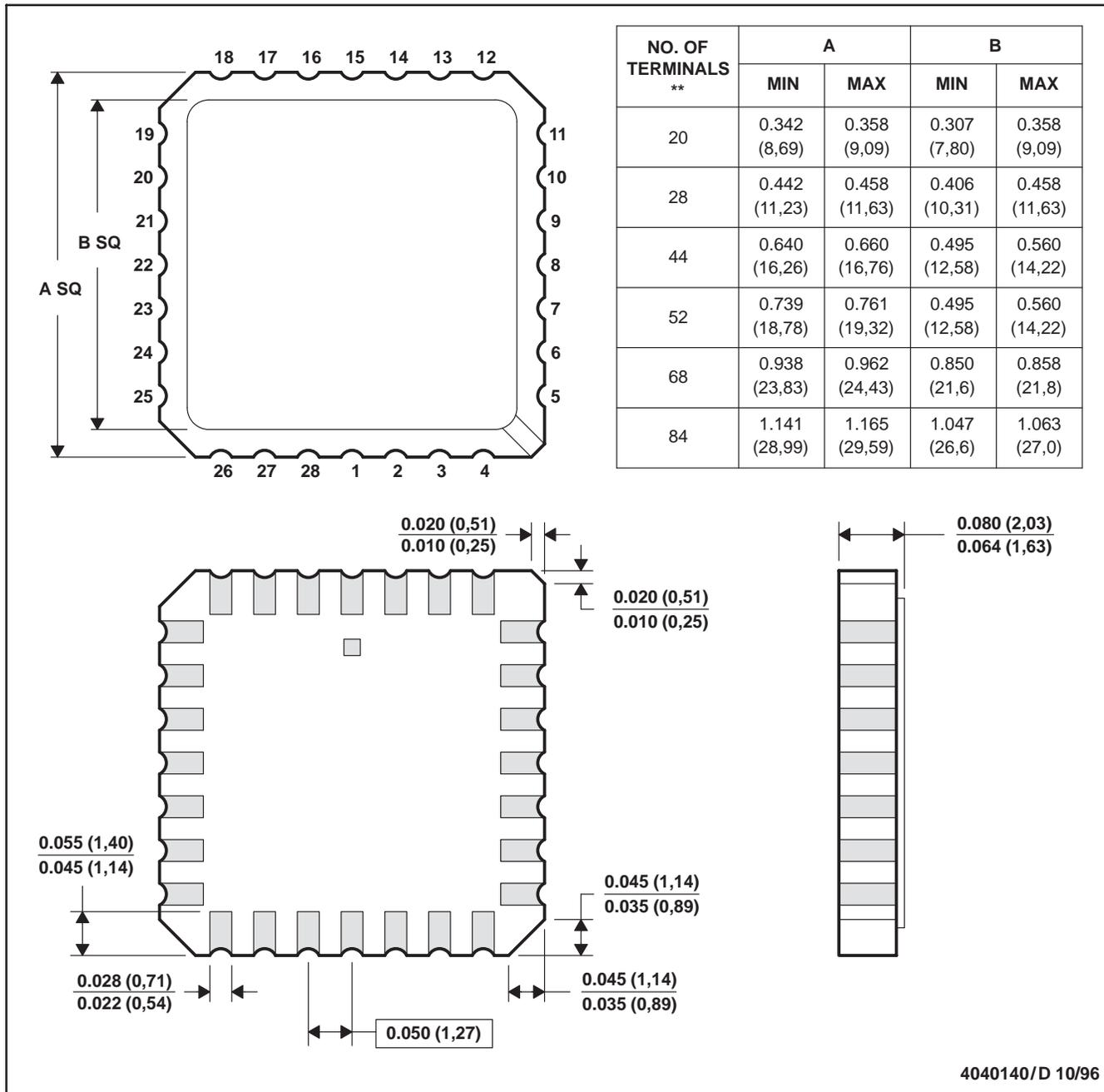
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

4040140 / D 10/96

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a metal lid.
         D.   The terminals are gold plated.
         E.   Falls within JEDEC MS-004

N (R−PDIP−T**)

16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

$\dfrac{0.260\ (6,60)}{0.240\ (6,10)}$

1   8

$\dfrac{0.070\ (1,78)}{0.045\ (1,14)}$ /D\

$\dfrac{0.045\ (1,14)}{0.030\ (0,76)}$ /D\

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

$\dfrac{0.021\ (0,53)}{0.015\ (0,38)}$

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option /D\

$\dfrac{0.325\ (8,26)}{0.300\ (7,62)}$

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E   12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
      /C\ Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
      /D\ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R−PDSO−G14)   PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

14   8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1   7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/F   07/2004

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−012 variation AB.

NS (R-PDSO-G)**   PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03
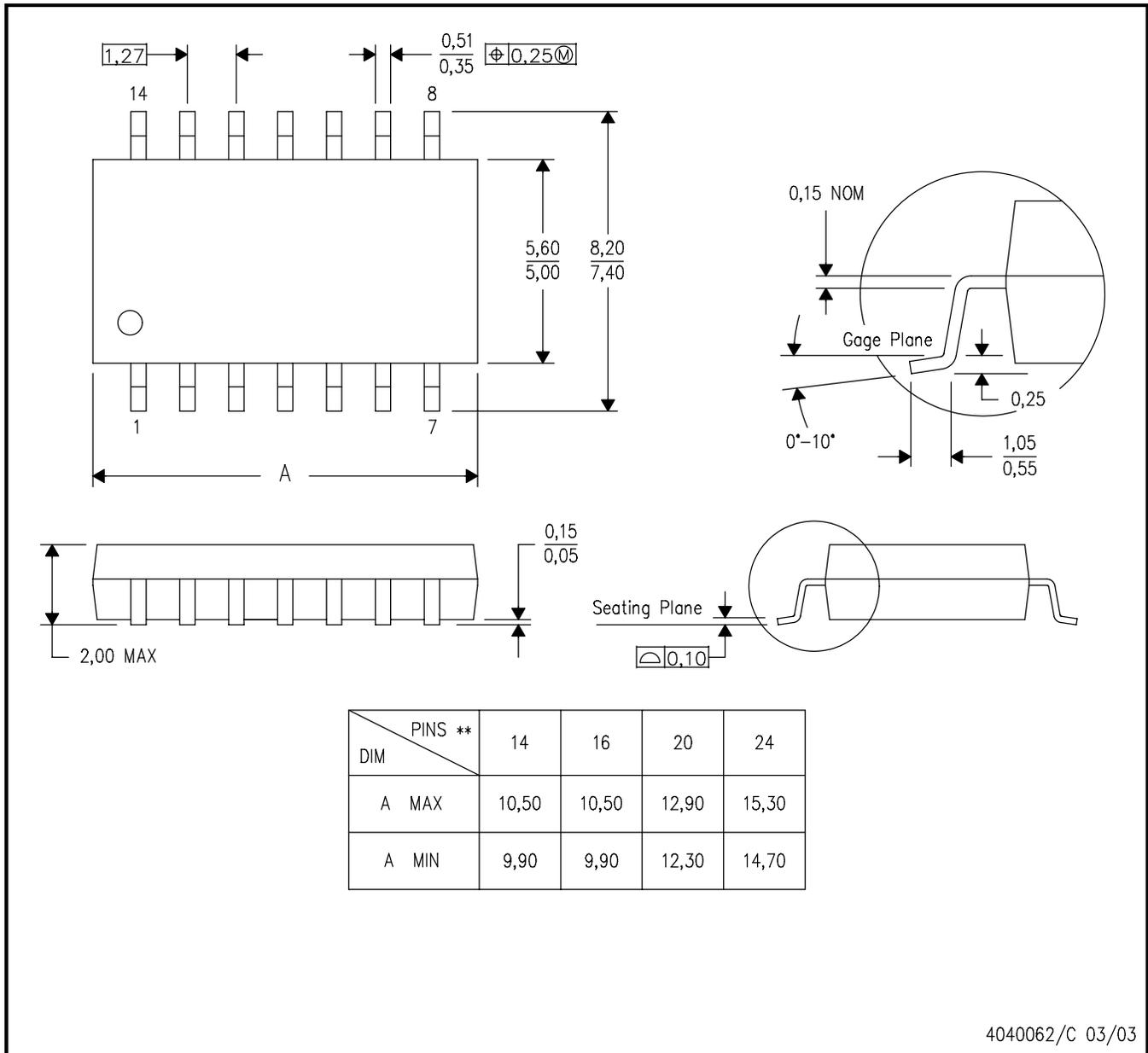
NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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