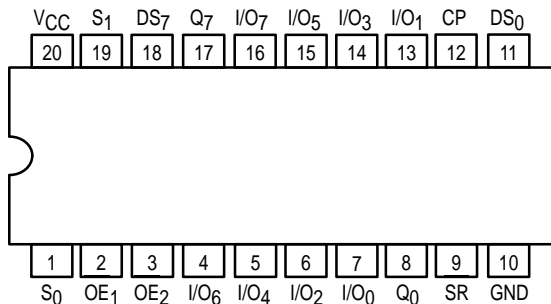# MOTOROLA

# 8-BIT SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUTS

The SN54/74LS323 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Its function is similar to the SN54/74LS299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate inputs and outputs are provided for flip-flops $Q_0$ and $Q_7$ to allow easy cascading.

Four operation modes are possible: hold (store), shift left, shift right, and parallel load. All modes are activated on the LOW-to-HIGH transition of the Clock.

- Common I/O for Reduced Pin Count
- Four Operation Modes: Shift Left, Shift Right, Parallel Load and Store
- Separate Continuous Inputs and Outputs from $Q_0$ and $Q_7$ Allow Easy Cascading
- Fully Synchronous Reset
- 3-State Outputs for Bus Oriented Applications
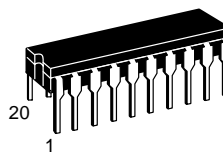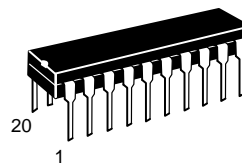- Input Clamp Diodes Limit High-Speed Termination Effects
- ESD > 3500 Volts

## SN54/74LS323

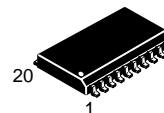### 8-BIT SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUTS

**LOW POWER SCHOTTKY**

**J SUFFIX**
CERAMIC
CASE 732-03

**N SUFFIX**
PLASTIC
CASE 738-03

**DW SUFFIX**
SOIC
CASE 751D-03

### ORDERING INFORMATION

SN54LSXXXJ    Ceramic
SN74LSXXXN    Plastic
SN74LSXXXDW  SOIC

## CONNECTION DIAGRAM DIP (TOP VIEW)

| $V_{CC}$ | $S_1$ | $DS_7$ | $Q_7$ | $I/O_7$ | $I/O_5$ | $I/O_3$ | $I/O_1$ | CP | $DS_0$ |
|---|---|---|---|---|---|---|---|---|---|
| 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 |

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|
| $S_0$ | $\overline{OE_1}$ | $\overline{OE_2}$ | $I/O_6$ | $I/O_4$ | $I/O_2$ | $I/O_0$ | $Q_0$ | SR | GND |

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

## PIN NAMES

| | | | |
|---|---|---|---|
| CP | Clock Pulse (active positive going edge) Input | | |
| $DS_0$ | Serial Data Input for Right Shift | | |
| $DS_7$ | Serial Data Input for Left Shift | | |
| $I/O_n$ | Parallel Data Input or | | |
| | Parallel Output (3-State) (Note c) | | |
| $\overline{OE_1}, \overline{OE_2}$ | 3-State Output Enable (active LOW) Inputs | | |
| $Q_0, Q_7$ | Serial Outputs (Note b) | | |
| $\underline{S_0}, S_1$ | Mode Select Inputs | | |
| SR | Synchronous Reset (active LOW) Input | | |

**LOADING** (Note a)

| | HIGH | LOW |
|---|---|---|
| CP | 0.5 U.L. | 0.25 U.L. |
| $DS_0$ | 0.5 U.L. | 0.25 U.L. |
| $DS_7$ | 0.5 U.L. | 0.25 U.L. |
| $I/O_n$ | 1.0 U.L. | 0.5 U.L. |
| | 65 (25) U.L. | 15 (7.5) U.L. |
| $\overline{OE_1}, \overline{OE_2}$ | 0.5 U.L. | 0.25 U.L. |
| $Q_0, Q_7$ | 10 U.L. | 5 (2.5) U.L. |
| $S_0, S_1$ | 1 U.L. | |
| SR | 0.5 U.L. | 0.25 U.L. |

NOTES:
a) 1 TTL LOAD = 40 µA HIGH/1.6 mA LOW.
b) The output LOW drive factor is 2.5 U.L for Military (54) and 5 U.L. for Commercial Temperature Ranges.
c) The output LOW drive factor is 7.5 U.L for Military (54) and 15 U.L. for Commercial Temperature Ranges.
   The output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial Temperature Ranges.

# SN54/74LS323

**LOGIC DIAGRAM**
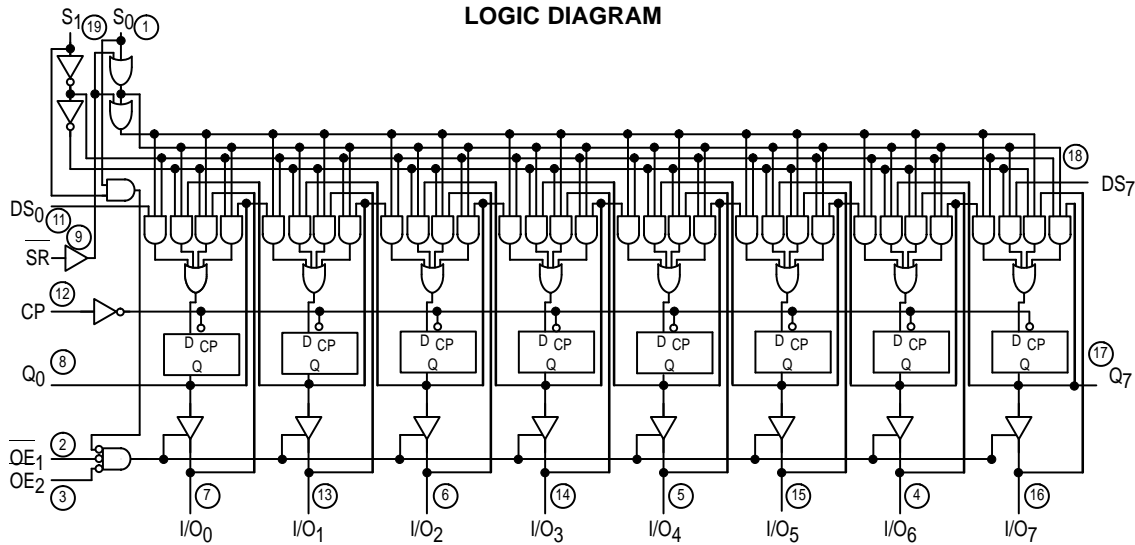


## FUNCTIONAL DESCRIPTION

The logic diagram and truth table indicate the functional characteristics of the SN54/74LS323 Universal Shift/Storage Register. This device is similar in operation to the SN54/74LS299 except for synchronous reset. A partial list of the common features are described below:

1. They use eight D-type edge-triggered flip-flops that respond only to the LOW-to-HIGH transition of the Clock (CP). The only timing restriction, therefore, is that the mode control ($S_0$, $S_1$) and data inputs ($DS_0$, $DS_7$, $I/O_0$–$I/O_7$) may be stable at least a setup time prior to the positive transition of the Clock Pulse.

2. When $S_0 = S_1 = 1$, $I/O_0$–$I/O_7$ are parallel inputs to flip-flops $Q_0$–$Q_7$ respectively, and the outputs of $Q_0$–$Q_7$ are in the high impedance state regardless of the state of $OE_1$ or $OE_2$.

An important unique feature of the SN54/74LS323 is a fully Synchronous Reset that requires only to be stable at least one setup time prior to the positive transition of the Clock Pulse.

**TRUTH TABLE**

| INPUTS | | | | | | | | RESPONSE |
|---|---|---|---|---|---|---|---|---|
| SR | $S_1$ | $S_0$ | $OE_1$ | $OE_2$ | CP | $DS_0$ | $DS_7$ | |
| L<br>L<br>L | X<br>X<br>H | X<br>X<br>H | H<br>X<br>X | X<br>H<br>X | ⌐<br>⌐<br>⌐ | X<br>X<br>X | X<br>X<br>X | Synchronous Reset; $Q_0 = Q_7$ = LOW<br>I/O voltage undetermined |
| L<br>L | L<br>X | X<br>L | L<br>L | L<br>L | ⌐<br>⌐ | X<br>X | X<br>X | Synchronous Reset; $Q_0 = Q_7$ = LOW<br>I/O voltage LOW |
| H<br>H | L<br>L | H<br>H | X<br>L | X<br>L | ⌐<br>⌐ | D<br>D | X<br>X | Shift Right; D→$Q_0$; $Q_0$→$Q_1$; etc.<br>Shift Right; D→$Q_0$ & $I/O_0$; $Q_0$→$Q_1$ & $I/O_1$; etc. |
| H<br>H | H<br>H | L<br>L | X<br>L | X<br>L | ⌐<br>⌐ | X<br>X | D<br>D | Shift Left; D→$Q_7$; $Q_7$→$Q_6$; etc.<br>Shift Left; D→$Q_7$ & $I/O_7$; $Q_7$→$Q_6$ & $I/O_6$; etc. |
| H | H | H | X | X | ⌐ | X | X | Parallel Load $I/O_n$→$Q_n$ |
| H<br>H | L<br>L | L<br>L | H<br>X | X<br>H | X<br>X | X<br>X | X<br>X | Hold; I/O Voltage Undetermined |
| H | L | L | L | L | X | X | X | Hold; $I/O_n = Q_n$ |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

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# SN54/74LS323

## GUARANTEED OPERATING RANGES

| Symbol | Parameter | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 54 | 4.5 | 5.0 | 5.5 | V |
| | | | 74 | 4.75 | 5.0 | 5.25 | |
| $T_A$ | Operating Ambient Temperature Range | | 54 | −55 | 25 | 125 | °C |
| | | | 74 | 0 | 25 | 70 | |
| $I_{OH}$ | Output Current — High | $Q_0$, $Q_7$ | 54, 74 | | | −0.4 | mA |
| $I_{OL}$ | Output Current — Low | $Q_0$, $Q_7$ | 54 | | | 4.0 | mA |
| | | $Q_0$, $Q_7$ | 74 | | | 8.0 | |
| $I_{OH}$ | Output Current — High | $I/O_0$−$I/O_7$ | 54 | | | −1.0 | mA |
| | | $I/O_0$−$I/O_7$ | 74 | | | −2.6 | |
| $I_{OL}$ | Output Current — Low | $I/O_0$−$I/O_7$ | 54 | | | 12 | mA |
| | | $I/O_0$−$I/O_7$ | 74 | | | 24 | |

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol | Parameter | | Limits | | | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | | |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | 54 | | | 0.7 | V | Guaranteed Input LOW Voltage for All Inputs | |
| | | 74 | | | 0.8 | | | |
| $V_{IK}$ | Input Clamp Diode Voltage | | | −0.65 | −1.5 | V | $V_{CC}$ = MIN, $I_{IN}$ = −18 mA | |
| $V_{OH}$ | Output HIGH Voltage $I/O_0$−$I/O_7$ | 54 | 2.4 | 3.2 | | V | $V_{CC}$ = MIN, $I_{OH}$ = MAX | |
| | | 74 | 2.4 | 3.1 | | V | | |
| $V_{OH}$ | Output HIGH Voltage $Q_0$, $Q_7$ | 54 | 2.5 | 3.4 | | V | $V_{CC}$ = MIN, $I_{OH}$ = MAX | |
| | | 74 | 2.7 | 3.4 | | V | | |
| $V_{OL}$ | Output LOW Voltage $I/O_0$−$I/O_7$ | 54, 74 | | 0.25 | 0.4 | V | $I_{OL}$ = 12 mA | $V_{CC}$ = $V_{CC}$ MIN, $V_{IN}$ = $V_{IL}$ or $V_{IH}$ per Truth Table |
| | | 74 | | 0.35 | 0.5 | V | $I_{OL}$ = 24 mA | |
| $V_{OL}$ | Output LOW Voltage $Q_0$−$Q_7$ | 54, 74 | | | 0.4 | V | $I_{OL}$ = 4.0 mA | $V_{CC}$ = $V_{CC}$ MIN, $V_{IN}$ = $V_{IL}$ or $V_{IH}$ per Truth Table |
| | | 74 | | | 0.5 | V | $I_{OL}$ = 8.0 mA | |
| $I_{OZH}$ | Output Off Current HIGH $I/O_0$−$I/O_7$ | | | | 40 | µA | $V_{CC}$ = MAX, $V_{OUT}$ = 2.7 V | |
| $I_{OZL}$ | Output Off Current LOW $I/O_0$−$I/O_7$ | | | | −400 | µA | $V_{CC}$ = MAX, $V_{OUT}$ = 0.4 V | |
| $I_{IH}$ | Input HIGH Current | Others | | | 20 | µA | $V_{CC}$ = MAX, $V_{IN}$ = 2.7 V | |
| | | $S_0$, $S_1$, $I/O_0$−$I/O_7$ | | | 40 | µA | | |
| | | Others | | | 0.1 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 7.0 V | |
| | | $S_0$, $S_1$ | | | 0.2 | mA | | |
| | | $I/O_0$−$I/O_7$ | | | 0.1 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 5.5 V | |
| $I_{IL}$ | Input LOW Current | Others | | | −0.4 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 0.4 V | |
| | | $S_0$, $S_1$ | | | −0.8 | mA | | |
| $I_{OS}$ | Short Circuit Current (Note 1) | $Q_0$, $Q_7$ | −20 | | −100 | mA | $V_{CC}$ = MAX | |
| | | $I/O_0$−$I/O_7$ | −30 | | −130 | mA | $V_{CC}$ = MAX | |
| $I_{CC}$ | Power Supply Current | | | | 53 | mA | $V_{CC}$ = MAX | |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

FAST AND LS TTL DATA

# SN54/74LS323

## AC CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|--------|-----------|-----|-----|-----|------|-----------------|
| $f_{MAX}$ | Maximum Clock Frequency | 25 | 35 | | MHz | $C_L = 15$ pF |
| $t_{PHL}$ $t_{PLH}$ | Propagation Delay, Clock to $Q_0$ or $Q_7$ | | 26 22 | 39 33 | ns | |
| $t_{PHL}$ $t_{PLH}$ | Propagation Delay, Clock to $I/O_0 - I/O_7$ | | 25 17 | 39 25 | ns | $C_L = 45$ pF, $R_L = 667$ Ω |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time | | 14 20 | 21 30 | ns | |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time | | 10 10 | 15 15 | ns | $C_L = 5.0$ pF |

## AC SETUP REQUIREMENTS ($T_A = 25°C$, $V_{CC} = 5.0$ V)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|--------|-----------|-----|-----|-----|------|-----------------|
| $t_W$ | Clock Pulse Width HIGH | 25 | | | ns | |
| $t_W$ | Clock Pulse Width LOW | 15 | | | ns | |
| $t_W$ | Clear Pulse Width LOW | 20 | | | ns | |
| $t_S$ | Data Setup Time | 20 | | | ns | |
| $t_S$ | Select Setup Time | 35 | | | ns | $V_{CC} = 5.0$ V |
| $t_h$ | Data Hold Time | 0 | | | ns | |
| $t_h$ | Select Hold Time | 10 | | | ns | |
| $t_{rec}$ | Recovery Time | 20 | | | ns | |

# SN54/74LS323

**3-STATE WAVEFORMS**
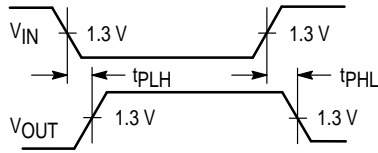


**Figure 1**
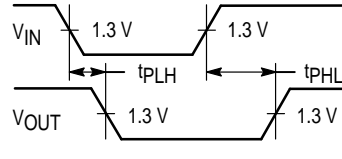


**Figure 2**
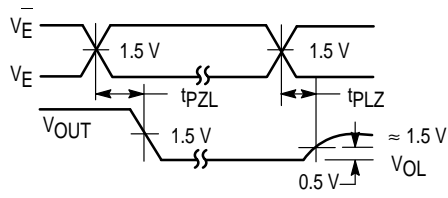


**Figure 3**
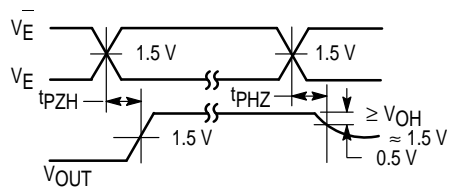


**Figure 4**

**AC LOAD CIRCUIT**
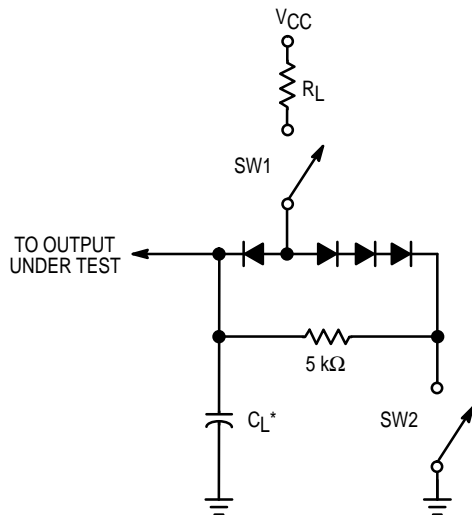


\* Includes Jig and Probe Capacitance.

**Figure 5**

**SWITCH POSITIONS**

| SYMBOL | SW1 | SW2 |
|---|---|---|
| $t_{PZH}$ | Open | Closed |
| $t_{PZL}$ | Closed | Open |
| $t_{PLZ}$ | Closed | Closed |
| $t_{PHZ}$ | Closed | Closed |