



4 x 4 REGISTER FILE OPEN-COLLECTOR

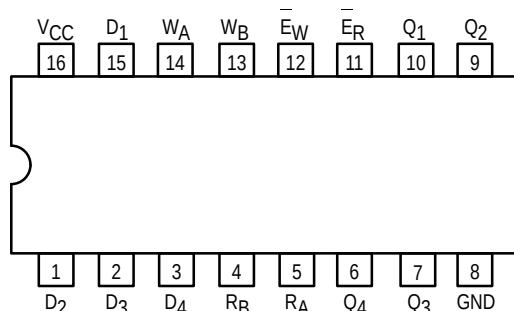
The TTL/MSI SN54/74LS170 is a high-speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

Open-collector outputs make it possible to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

The SN54/74LS670 provides a similar function to this device but it features 3-state outputs.

- Simultaneous Read/Write Operation
- Expandable to 512 Words of n-Bits
- Typical Access Time of 20 ns
- Low Leakage Open-Collector Outputs for Expansion
- Typical Power Dissipation of 125 mW

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version
has the same pinouts
(Connection Diagram) as
the Dual In-Line Package.

PIN NAMES

D ₁ –D ₄	Data Inputs
W _A , W _B	Write Address Inputs
E _W	Write Enable (Active LOW) Input
R _A , R _B	Read Address Inputs
E _R	Read Enable (Active LOW) Input
Q ₁ –Q ₄	Outputs (Note b)

LOADING (Note a)

	HIGH	LOW
D ₁ –D ₄	0.5 U.L.	0.25 U.L.
W _A , W _B	0.5 U.L.	0.25 U.L.
E _W	1.0 U.L.	0.5 U.L.
R _A , R _B	0.5 U.L.	0.25 U.L.
E _R	1.0 U.L.	0.5 U.L.
Q ₁ –Q ₄	Open-Collector	5 (2.5) U.L.

NOTES:

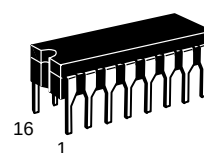
a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74)
Temperature Ranges. The Output HIGH drive must be supplied by an external resistor to V_{CC}.

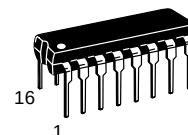
SN54/74LS170

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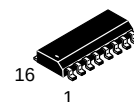
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-08



N SUFFIX
PLASTIC
CASE 648-08

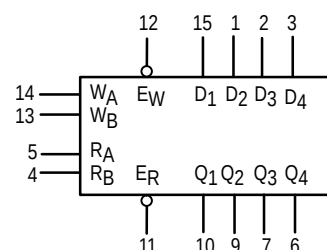


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

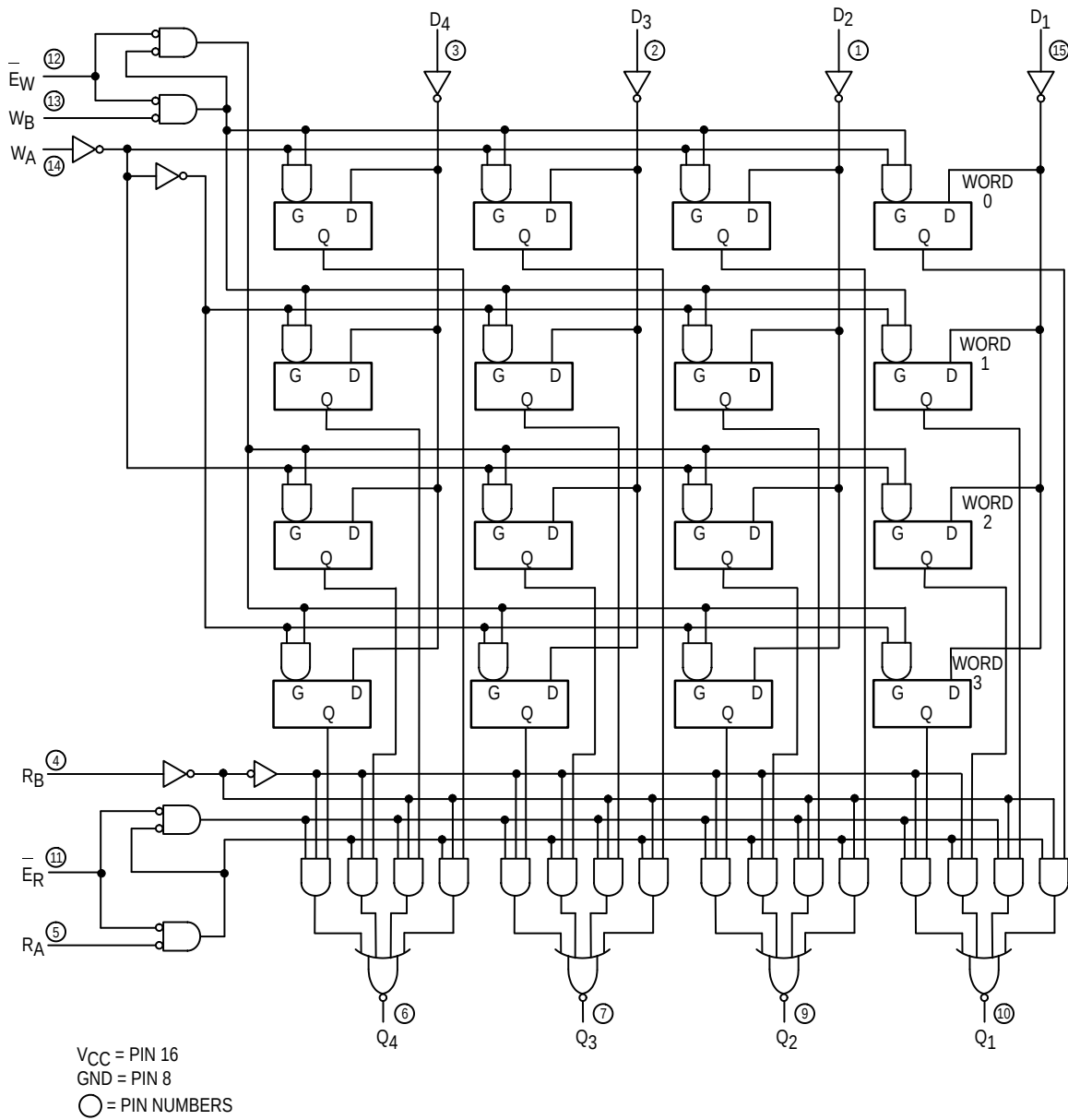
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN54/74LS170

LOGIC DIAGRAM



SN54/74LS170

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

WRITE INPUTS			WORD			
W_B	W_A	E_W	0	1	2	3
L	L	L	Q = D	Q ₀	Q ₀	Q ₀
L	H	L	Q ₀	Q = D	Q ₀	Q ₀
H	L	L	Q ₀	Q ₀	Q = D	Q ₀
H	H	L	Q ₀	Q ₀	Q ₀	Q = D
X	X	H	Q ₀	Q ₀	Q ₀	Q ₀

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	E_R	Q ₁	Q ₂	Q ₃	Q ₄
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

NOTES: A. H = HIGH Level, L = LOW Level, X = Irrelevant.

B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

C. Q₀ = the level of Q before the indicated input conditions were established.

D. W_{0B1} = The first bit of word 0, etc.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
V _{OH}	Output Voltage — High	54, 74			5.5	V
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
I _{OH}	Output HIGH Current	54, 74			100	μA	V _{CC} = MIN, V _{OH} = MAX
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA
		74		0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current Any $\overline{D}$, R, W E_R , E_W				20 40	μA	V _{CC} = MAX, V _{IN} = 2.4 V
	Any $\overline{D}$, R, W E_R , E_W				0.1 0.2	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current Any $\overline{D}$, R, W E_R , E_W				-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{CC}	Power Supply Current				40	mA	V _{CC} = MAX

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AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going E_R to Q Outputs		20 20	30 30	ns	Figure 1	$V_{CC} = 5.0\text{ V}$ $C_L = 15\text{ pF}$ $R_L = 2.0\text{ k}\Omega$
t_{PLH} t_{PHL}	Propagation Delay, R_A or R_B to Q Outputs		25 24	40 40	ns	Figure 2	
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going E_W to Q Outputs		30 26	45 40	ns	Figure 1	
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs to Q Outputs		30 22	45 35	ns	Figure 1	

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
t_W	Pulse Width, E_R , E_W	25			ns	$V_{CC} = 5.0\text{ V}$ $R_L = 2.0\text{ k}\Omega$	
t_S	Setup Time, Data to E_W	10			ns		
t_S	Setup Time, W_A , W_B to E_W	15			ns		
t_H	Hold Time, Data to E_W	15			ns		
t_H	Hold Time, W_A , W_B to E_W	5.0			ns		
t_{LATCH}	Latch Time	25			ns		

VOLTAGE WAVEFORMS

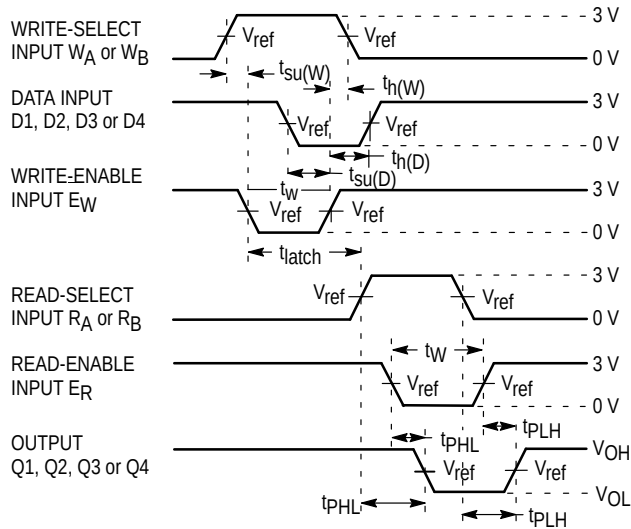


Figure 1

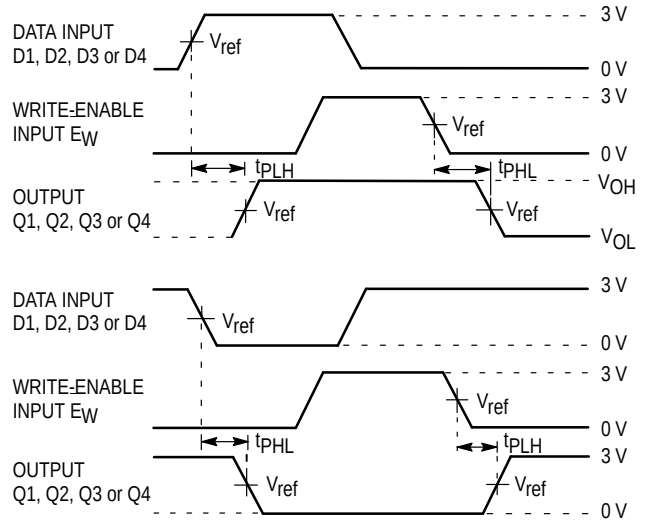


Figure 2