- **Qualification in Accordance With AEC-Q100†**
- **Qualified for Automotive Applications**
- **Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval**
- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 20-μA Max I$_{CC}$**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
- **True Logic**
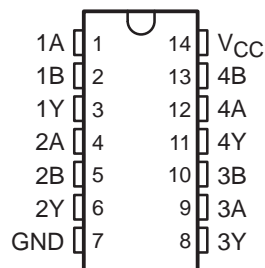
† Contact factory for details. Q100 qualification data available on request.

D OR PW PACKAGE
(TOP VIEW)

```
       ___ ___
 1A [ 1    14 ] V_CC
 1B [ 2    13 ] 4B
 1Y [ 3    12 ] 4A
 2A [ 4    11 ] 4Y
 2B [ 5    10 ] 3B
 2Y [ 6     9 ] 3A
GND [ 7     8 ] 3Y
```

description/ordering information

This device contains four independent 2-input exclusive-OR gates. They perform the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

ORDERING INFORMATION

T$_A$	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC – D	Reel of 2500	SN74HC86IDRQ1	HC86I
	TSSOP – PW	Reel of 2000	SN74HC86IPWRQ1	HC86I
−40°C to 125°C	SOIC – D	Reel of 2500	SN74HC86QDRQ1	HC86Q
	TSSOP – PW	Reel of 2000	SN74HC86QPWRQ1	HC86Q

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

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TEXAS INSTRUMENTS

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.
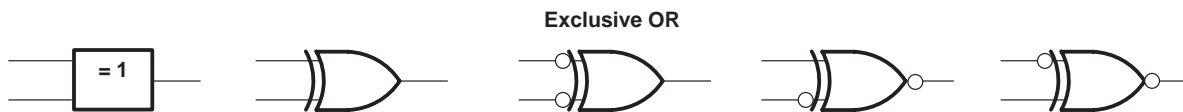
Exclusive OR

These are five equivalent exclusive-OR symbols valid for an 'HC86 gate in positive logic; negation may be shown at any two ports.

Logic Identity Element

The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

Even-Parity Element
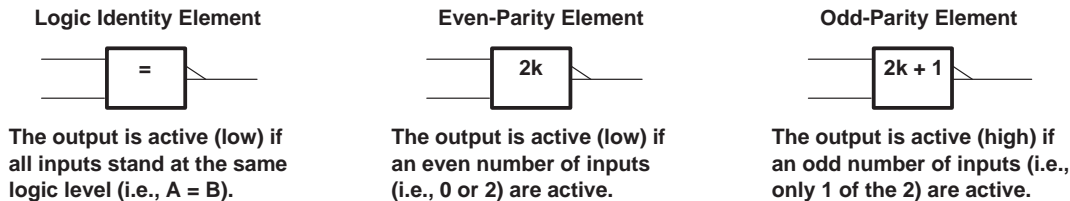

The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

Odd-Parity Element

The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) .... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±25 mA
Continuous current through V_{CC} or GND .... ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package .... 86°C/W
PW package .... 113°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature		−40		125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

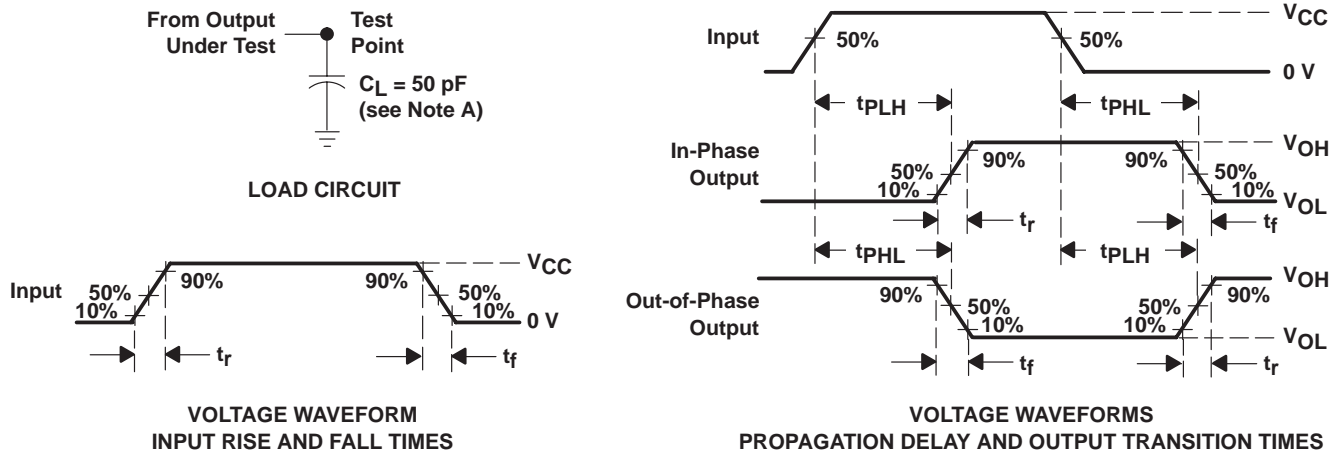| PARAMETER	TEST CONDITIONS		V_{CC}	T_A = −40°C TO 125°C		T_A = −40°C TO 85°C		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = −20 µA	2 V	1.9		1.9		V
			4.5 V	4.4		4.4		
			6 V	5.9		5.9		
		I_{OH} = −4 mA	4.5 V	3.7		3.84		
		I_{OH} = −5.2 mA	6 V	5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V		0.1		0.1	V
			4.5 V		0.1		0.1	
			6 V		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V		40		20	µA
C_i			2 V to 6 V		10		10	pF

TEXAS INSTRUMENTS

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = −40°C TO 125°C		T_A = −40°C TO 85°C		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		150		125	ns
			4.5 V		30		25	
			6 V		25		21	
t_t		Y	2 V		110		95	ns
			4.5 V		22		19	
			6 V		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	35	pF

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

VOLTAGE WAVEFORM INPUT RISE AND FALL TIMES

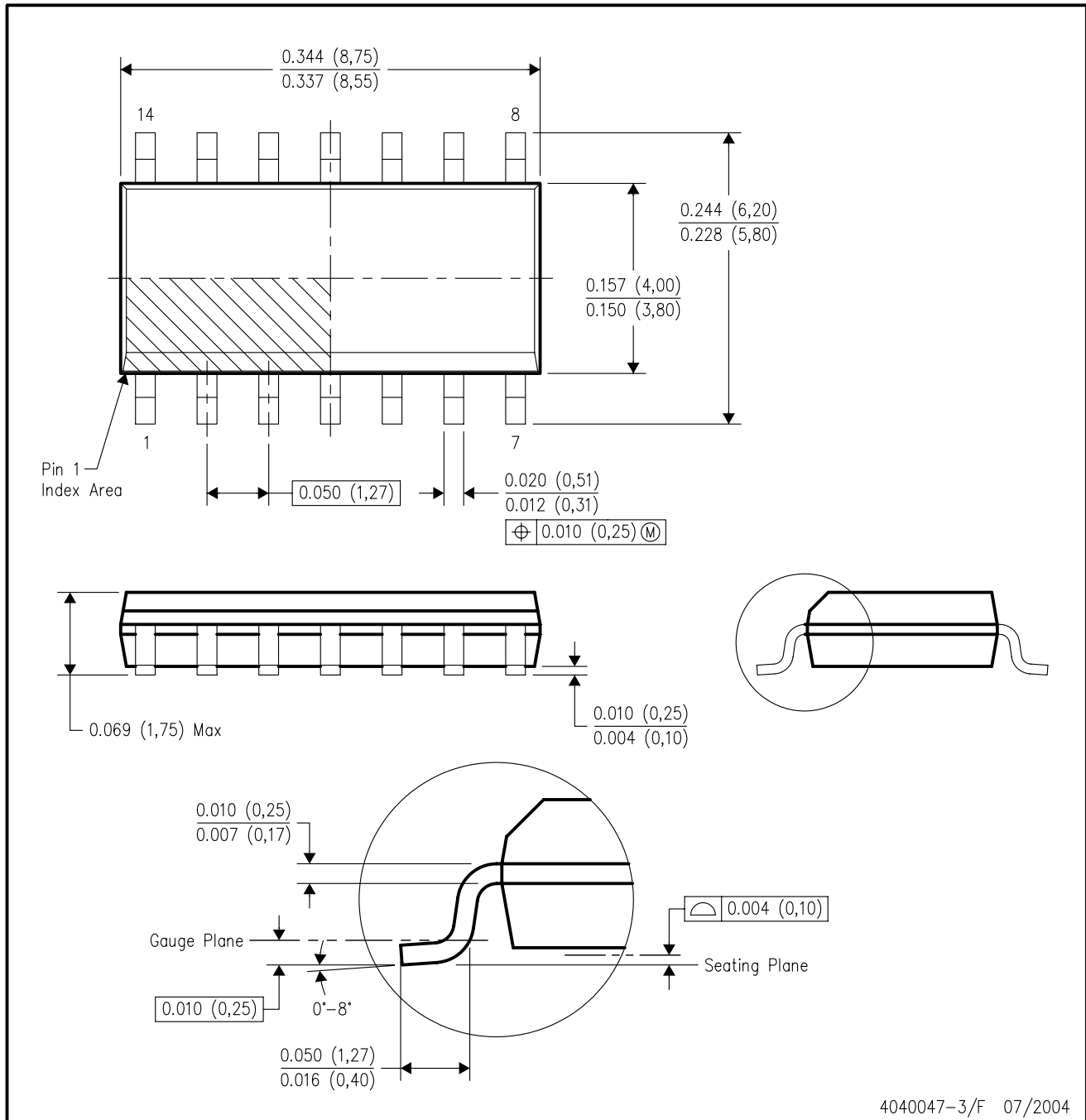**VOLTAGE WAVEFORMS PROPAGATION DELAY AND OUTPUT TRANSITION TIMES**

NOTES: A. C_L includes probe and test-fixture capacitance.
        B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
        C. The outputs are measured one at a time, with one input transition per measurement.
        D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

D (R−PDSO−G14) PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

14

8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1

7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/F 07/2004

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS−012 variation AB.

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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