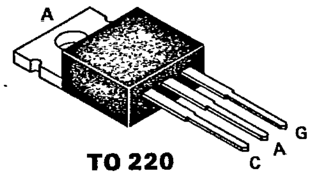
TAG SEMICONDUCTORS LTD

S0602BH – S0602NH SCR'S

6.0 A 200–800 V <200 μA

The S0602 series silicon controlled rectifiers are high performance glass passivated PNPN devices. These parts are intended for general purpose high voltage applications where gate sensitivity is required.



TO 220

Absolute Maximum Ratings $T_A = 25\,°C$ unless otherwise noted

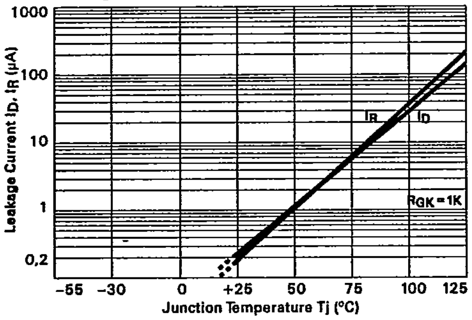
Parameter	Part Nr.	Symbol	Min.	Max.	Unit	Test Conditions
Repetitive Peak Off State Voltage	**S0602BH**	V_{DRM} V_{RRM}	200		V	$T_j = -40\,°C$ to $125\,°C$ $R_{GK} = 1\,K\Omega$
	S0602DH		400		V	
	S0602MH		600		V	
	S0602NH		800		V	
On-State Current		$I_{T(RMS)}$	6.0		A	All Conduction Angles $T_C = 85\,°C$
Average On-State Current		$I_{T(AV)}$	3.8		A	Half Cycle, $\Theta = 180°$, $T_C = 85\,°C$
Nonrept. On-State Current		I_{TSM}	65		A	Half Cycle, 60 Hz
Nonrept. On-State Current		I_{TSM}	60		A	Half Cycle, 50 Hz
Fusing Current		I^2t	18		A^2s	t = 10 ms, Half Cycle
Peak Reverse Gate Voltage		V_{GRM}	8		V	$I_{GR} = 50\,\mu A$
Peak Gate Current		I_{GM}	2		A	10μs max.
Peak Gate Dissipation		P_{GM}	5		W	10μs max.
Gate Dissipation		$P_{G(AV)}$	0.5		W	20 ms max.
Operating Temperature		T_j	−40	125	°C	
Storage Temperature		T_{stg}	−40	125	°C	
Soldering Temperature		T_{sld}		250	°C	1.6 mm from case, 10 s max.

Electrical Characteristics $T_A = 25\,°C$ unless otherwise noted

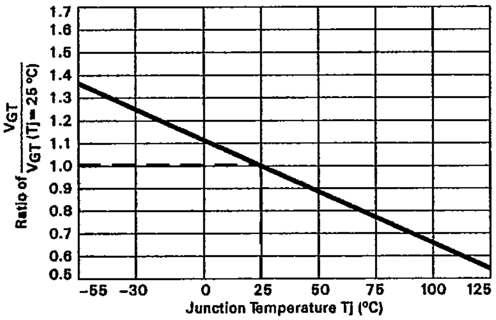
Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Off-State Leakage Current	I_{DRM}/I_{RRM}		0.5	mA	@$V_{DRM} + V_{RRM}$, $R_{GK} = 1\,K\Omega$, $T_j = 125\,°C$
Off-State Leakage Current	I_{DRM}/I_{RRM}		5	μA	@$V_{DRM} + V_{RRM}$, $R_{GK} = 1\,K\Omega$, $T_j = 25\,°C$
On-State Voltage	V_T		2.45	V	at $I_T = 12\,A$, $T_j = 25\,°C$
On-State Threshold Voltage	$V_{T(TO)}$		1.15	V	$T_j = 125\,°C$
On-State Slope Resistance	r_T		125	mΩ	$T_j = 125\,°C$
Gate Trigger Current	I_{GT}		200	μA	$V_D = 7\,V$
Gate Trigger Voltage	V_{GT}		2.0	V	$V_D = 7\,V$
Holding Current	I_H		10	mA	$R_{GK} = 1\,K\Omega$
Latching Current	I_L		20	mA	$R_{GK} = 1\,K\Omega$
Critical Rate of Voltage Rise	dv/dt	5		V/μs	$V_D = .67xV_{DRM}$ $R_{GK} = 1\,K\Omega$ $T_j = 125\,°C$
Critical Rate of Current Rise	di/dt	100		A/μs	$I_G = 10\,mA$ $di_G/dt = 0.1\,A/\mu s$ $T_j = 125\,°C$
Gate Controlled Delay Time	t_{gd}		500	ns	$I_G = 10\,mA$ $di_G/dt = 0.1\,A/\mu s$
Commutated Turn-Off Time	t_q		100	μs	$T_C = 85\,°C$ $V_D = .67xV_{DRM}$ $V_R = 35\,V$ $I_T = I_{T(AV)}$
Thermal Resistance junc. to case	$R_{\Theta jc}$		4	K/W	
Thermal Resistance junc. to amb.	$R_{\Theta ja}$		60	K/W	

Typical Characteristics S06 – Chips

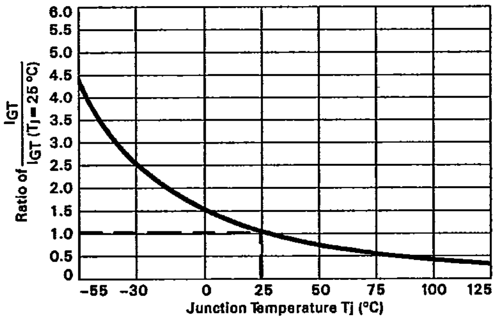
Leakage Current vs Junction Temperature (typical)



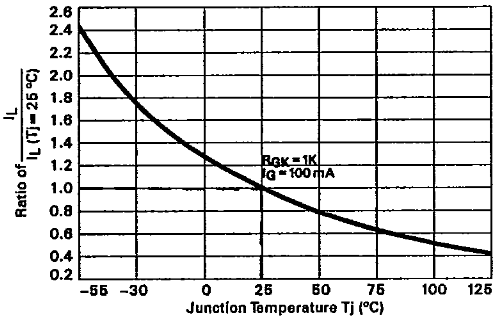
Normalized DC Gate Trigger Voltage vs Junction Temperature (typical)



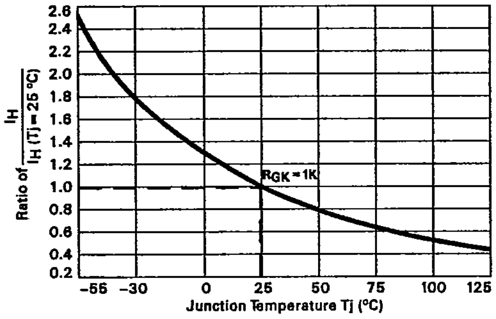
Normalized DC Gate Trigger Current vs Junction Temperature (typical)



Normalized DC Latching Current vs Junction Temperature (typical)

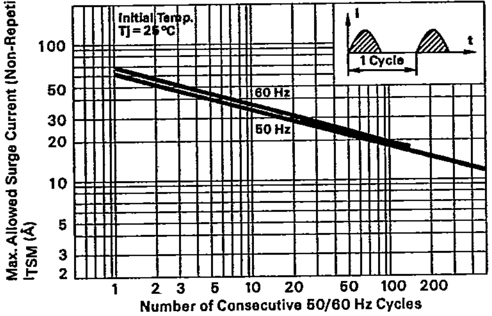


Normalized DC Holding Current vs Junction Temperature (typical)

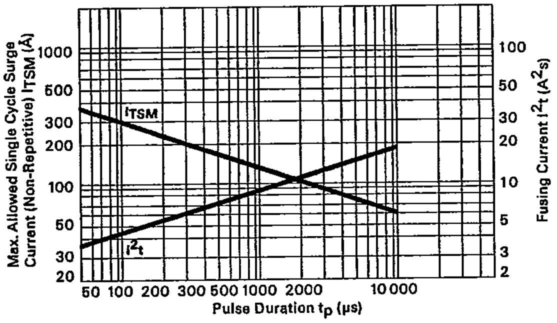


Typical Characteristics S06 – Packaged Parts

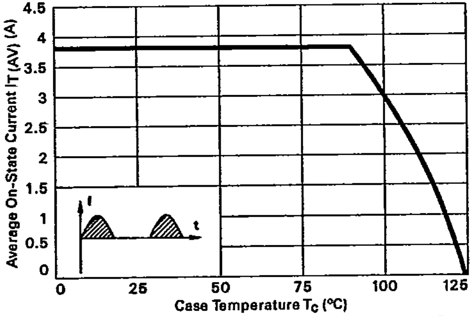
Max. Allowed Multi Cycle Surge (On-State) Current vs Number of Consecutive Cycles



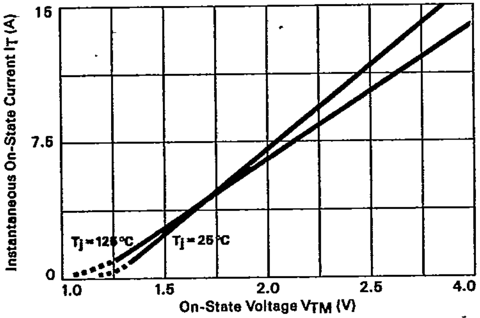
Max. Allowed Single Cycle Surge (On-State) Current vs Surge Current Duration



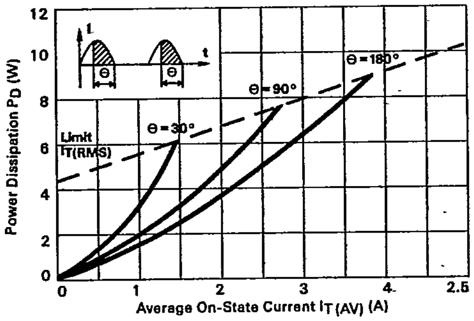
Average On-State Current vs Case Temperature



Instantaneous On-State Current vs On-State Voltage with Junction Temperature as Parameter



Power Dissipation vs Average On-State Current with Phase Conducting Angles as Parameter



Max. All. Power Dissip. vs Ambient Temp. with given Heatsink Thermal Resistances as Parameter