Dual Low Bias Current Precision Operational Amplifier

OP297

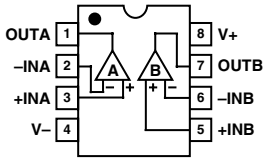
FEATURES

Low Offset Voltage: 50 μV Max
Low Offset Voltage Drift: 0.6 μV/°C Max
Very Low Bias Current: 100 pA Max
Very High Open-Loop Gain: 2000 V/mV Min
Low Supply Current (Per Amplifier): 625 μA Max
Operates From ±2 V to ±20 V Supplies
High Common-Mode Rejection: 120 dB Min
Pin Compatible to LT1013, AD706, AD708, OP221, LM158, and MC1458/1558 with Improved Performance

APPLICATIONS

Strain Gage and Bridge Amplifiers
High Stability Thermocouple Amplifiers
Instrumentation Amplifiers
Photo-Current Monitors
High Gain Linearity Amplifiers
Long-Term Integrators/Filters
Sample-and-Hold Amplifiers
Peak Detectors
Logarithmic Amplifiers
Battery-Powered Systems

PIN CONNECTIONS



GENERAL DESCRIPTION

The OP297 is the first dual op amp to pack precision performance into the space-saving, industry-standard, 8-lead SOIC package. Its combination of precision with low power and extremely low input bias current makes the dual OP297 useful in a wide variety of applications.

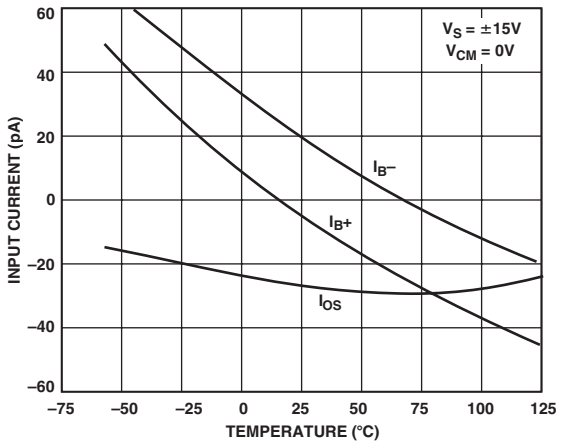


Figure 1. Low Bias Current over Temperature

Precision performance of the OP297 includes very low offset, under 50 μV, and low drift, below 0.6 μV/°C. Open-loop gain exceeds 2000 V/mV, ensuring high linearity in every application.

Errors due to common-mode signals are eliminated by the OP297's common-mode rejection of over 120 dB, which minimizes offset voltage changes experienced in battery-powered systems. Supply current of the OP297 is under 625 μA per amplifier, and the part can operate with supply voltages as low as ±2 V.

The OP297 uses a super-beta input stage with bias current cancellation to maintain picoamp bias currents at all temperatures. This is in contrast to FET input op amps whose bias currents start in the picoamp range at 25°C, but double for every 10°C rise in temperature, to reach the nanoamp range above 85°C. Input bias current of the OP297 is under 100 pA at 25°C and is under 450 pA over the military temperature range.

Combining precision, low power, and low bias current, the OP297 is ideal for a number of applications, including instrumentation amplifiers, log amplifiers, photodiode preamplifiers, and long-term integrators. For a single device, see the OP97; for a quad, see the OP497.

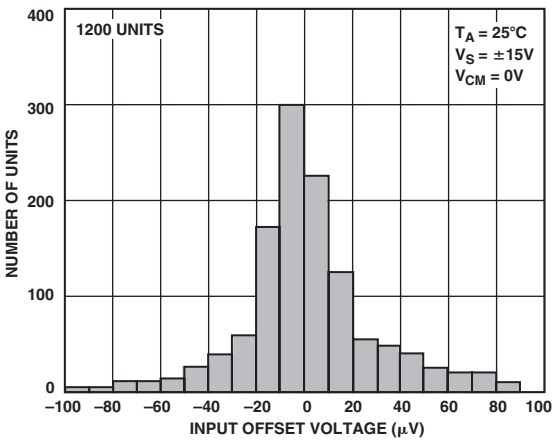


Figure 2. Very Low Offset

REV. E

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OP297–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP297E			OP297F			OP297G			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{OS}			25	50		50	100		80	200	µV
Long-Term Input Voltage Stability				0.1			0.1			0.1		µV/mo
Input Offset Current	I_{OS}	V_{CM} = 0 V		20	100		35	150		50	200	pA
Input Bias Current	I_B	V_{CM} = 0 V		20	±100		35	±150		50	±200	pA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz		0.5			0.5			0.5		µV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz		20			20			20		nV/√Hz
		f_O = 1000 Hz		17			17			17		nV/√Hz
Input Noise Current Density	i_n	f_O = 10 Hz		20			20			20		fA/√Hz
Input Resistance Differential Mode	R_{IN}			30			30			30		MΩ
Input Resistance Common-Mode	R_{INCM}			500			500			500		GΩ
Large-Signal Voltage Gain	A_{VO}	V_O = ±10 V, R_L = 2 kΩ	2000	4000		1500	3200		1200	3200		V/mV
Input Voltage Range*	V_{CM}		±13	±14		±13	±14		±13	±14		V
Common-Mode Rejection	CMRR	V_{CM} = ±13 V	120	140		114	135		114	135		dB
Power Supply Rejection	PSRR	V_S = ±2 V to ±20 V	120	130		114	125		114	125		dB
Output Voltage Swing	V_O	R_L = 10 kΩ	±13	±14		±13	±14		±13	±14		V
		R_L = 2 kΩ	±13	±13.7		±13	±13.7		±13	±13.7		V
Supply Current per Amplifier	I_{SY}	No Load		525	625		525	625		525	625	µA
Supply Voltage	V_S	Operating Range	±2		±20	±2		±20	±2		±20	V
Slew Rate	SR		0.05	0.15		0.05	0.15		0.05	0.15		V/µs
Gain Bandwidth Product	GBWP	A_V = +1		500			500			500		kHz
Channel Separation	CS	V_O = 20 V p-p, f_O = 10 Hz		150			150			150		dB
Input Capacitance	C_{IN}			3			3			3		pF

*Guaranteed by CMR test.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, –40°C ≤ T_A ≤ +85°C for OP297E/F/G, unless otherwise noted.)

Parameter	Symbol	Conditions	OP297E			OP297F			OP297G			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{OS}			35	100		80	300		110	400	µV
Average Input Offset Voltage Drift	TCV_{OS}			0.2	0.6		0.5	2.0		0.6	2.0	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0 V		50	450		80	750		80	750	pA
Input Bias Current	I_B	V_{CM} = 0 V		50	±450		80	±750		80	±750	pA
Large-Signal Voltage Gain	A_{VO}	V_O = ±10 V, R_L = 2 kΩ	1200	3200		1000	2500		800	2500		V/mV
Input Voltage Range*	V_{CM}		±13	±13.5		±13	±13.5		±13	±13.5		V
Common-Mode Rejection	CMRR	V_{CM} = ±13	114	130		108	130		108	130		dB
Power Supply Rejection	PSRR	V_S = ±2.5 V to ±20 V	114	0.15		108	0.15		108	0.3		dB
Output Voltage Swing	V_O	R_L = 10 kΩ	±13	±13.4		±13	±13.4		±13	±13.4		V
Supply Current per Amplifier	I_{SY}	No Load		550	750		550	750		550	750	µA
Supply Voltage	V_S	Operating Range	±2.5		±20	±2.5		±20	±2.5		±20	V

*Guaranteed by CMR test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±20 V
Input Voltage[2] . . . . . ±20 V
Differential Input Voltage[2] . . . . . 40 V
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
  Z Package . . . . . –65°C to +175°C
  P, S Packages . . . . . –65°C to +150°C
Operating Temperature Range
  OP297E (Z) . . . . . –40°C to +85°C
  OP297F, OP297G (P, S) . . . . . –40°C to +85°C
Junction Temperature
  Z Package . . . . . –65°C to +175°C
  P, S Packages . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C

Package Types	θ_{JA}[3]	θ_{JC}	Unit
8-Lead CERDIP (Z)	134	12	°C/W
8-Lead PDIP (P)	96	37	°C/W
8-Lead SOIC (S)	150	41	°C/W

NOTES
[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2] For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
[3] θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for CERDIP and PDIP, packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
OP297EZ	–40°C to +85°C	8-Lead CERDIP	Q-8
OP297FP	–40°C to +85°C	8-Lead PDIP	N-8
OP297FS	–40°C to +85°C	8-Lead SOIC	R-8
OP297FS-REEL	–40°C to +85°C	8-Lead SOIC	R-8
OP297FS-REEL7	–40°C to +85°C	8-Lead SOIC	R-8
OP297GP	–40°C to +85°C	8-Lead PDIP	N-8
OP297GS	–40°C to +85°C	8-Lead SOIC	R-8
OP297GS-REEL	–40°C to +85°C	8-Lead SOIC	R-8
OP297GS-REEL7	–40°C to +85°C	8-Lead SOIC	R-8

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP297 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

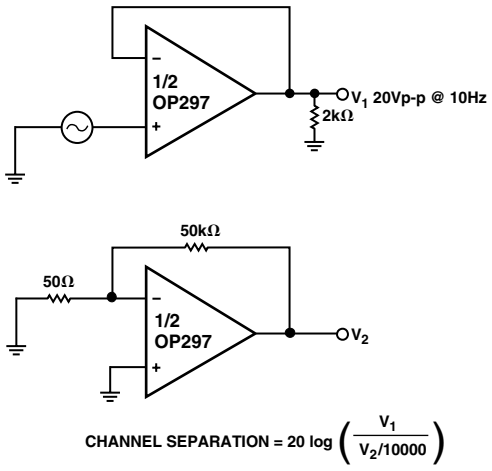
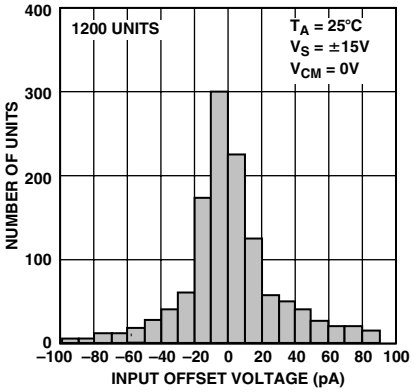
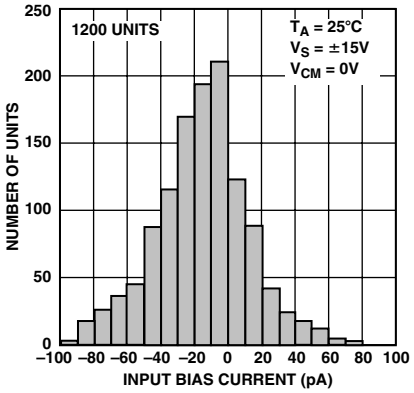


Figure 3. Channel Separation Test Circuit

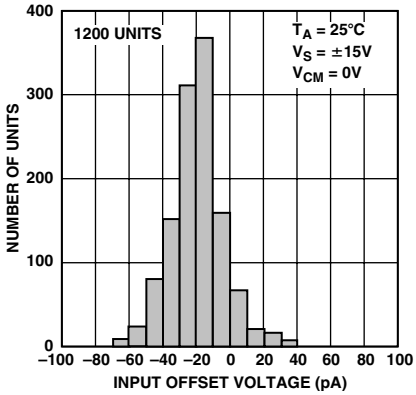
OP297–Typical Performance Characteristics



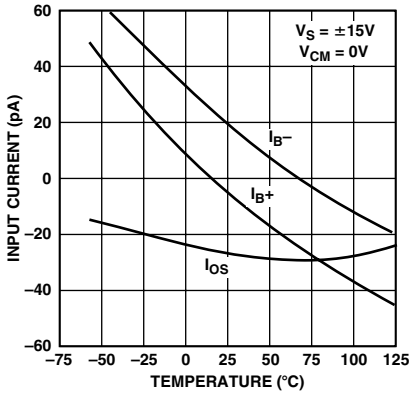
TPC 1. Typical Distribution of Input Offset Voltage



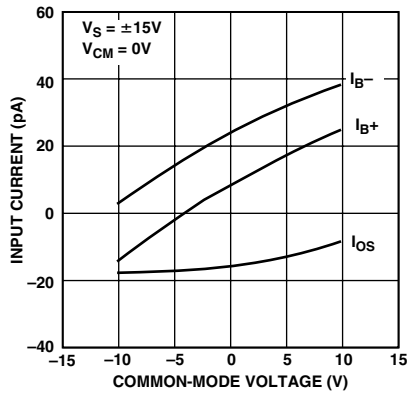
TPC 2. Typical Distribution of Input Bias Current



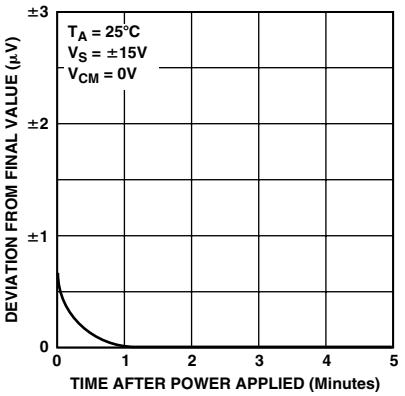
TPC 3. Typical Distribution of Input Offset Current



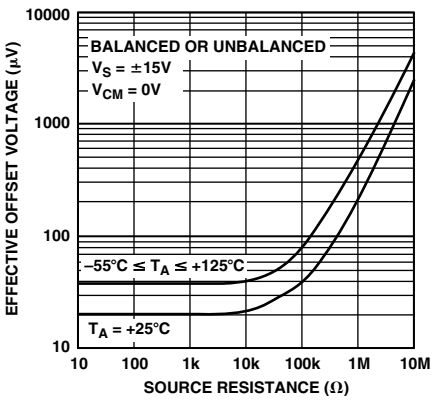
TPC 4. Input Bias, Offset Current vs. Temperature



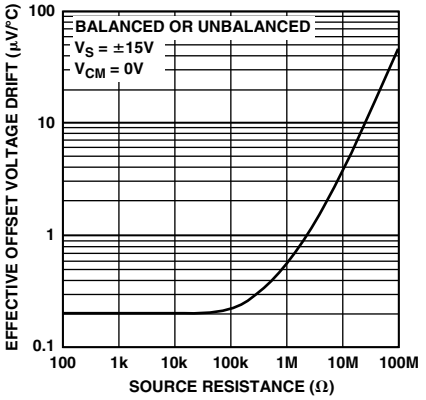
TPC 5. Input Bias, Offset Current vs. Common-Mode Voltage



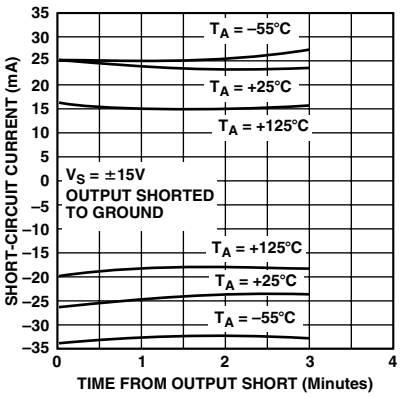
TPC 6. Input Offset Voltage Warm-Up Drift



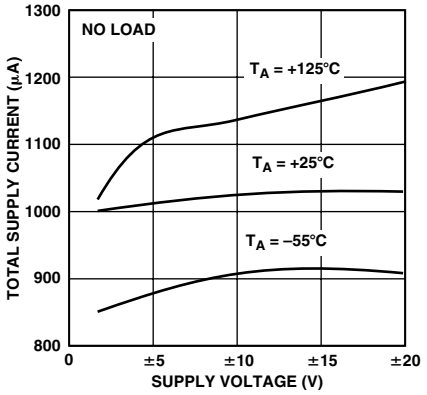
TPC 7. Effective Offset Voltage vs. Source Resistance



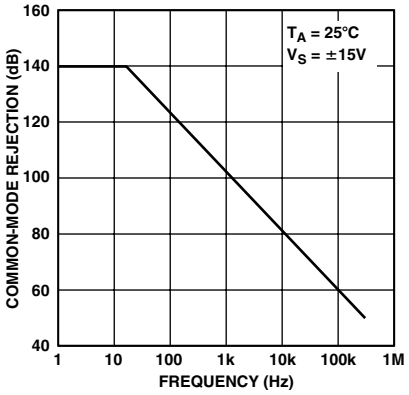
TPC 8. Effective TCV_{OS} vs. Source Resistance



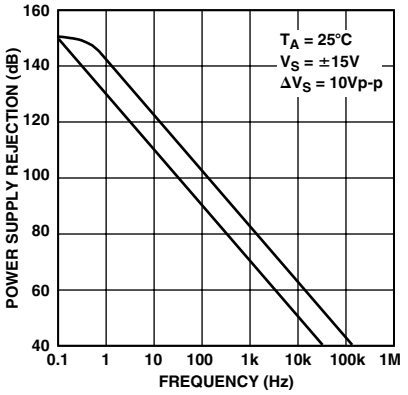
TPC 9. Short Circuit Current vs. Time, Temperature



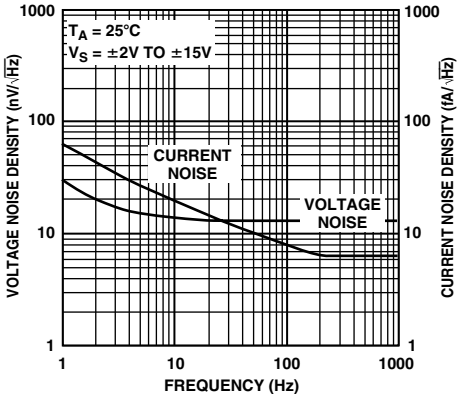
TPC 10. Total Supply Current vs. Supply Voltage



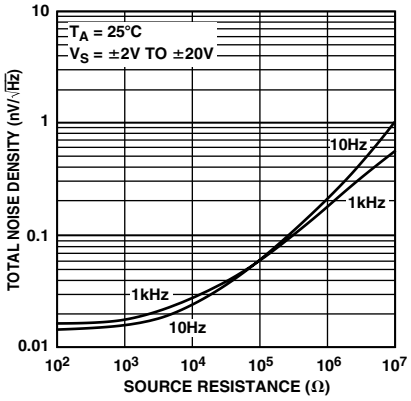
TPC 11. Common-Mode Rejection Frequency



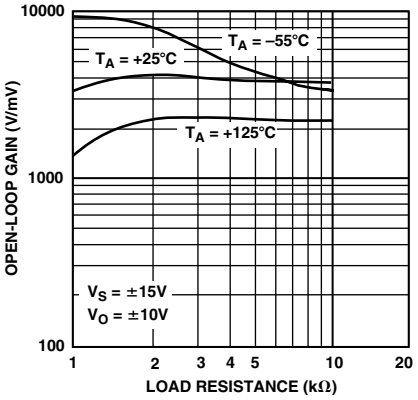
TPC 12. Power Supply Rejection vs. Frequency



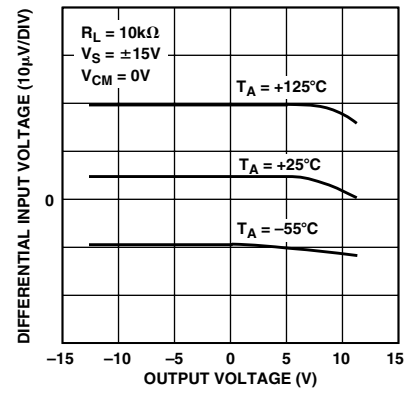
TPC 13. Voltage Noise Density and Current Noise Density vs. Frequency



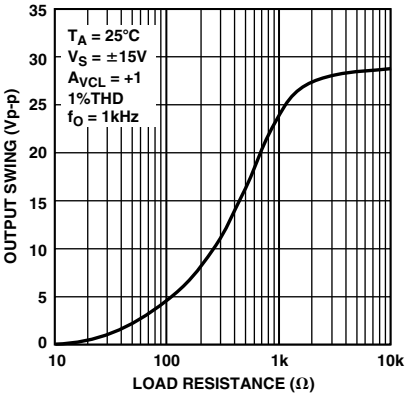
TPC 14. Total Noise Density vs. Source Resistance



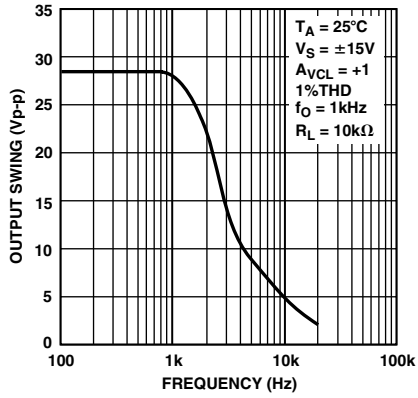
TPC 15. Open-Loop Gain vs. Load Resistance



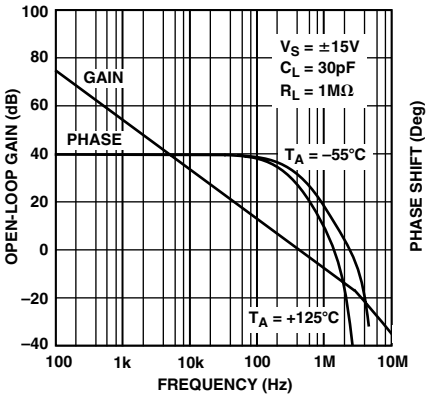
TPC 16. Differential Input Voltage vs. Output Voltage



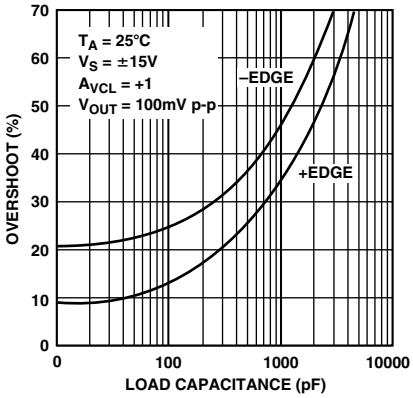
TPC 17. Output Swing vs. Load Resistance



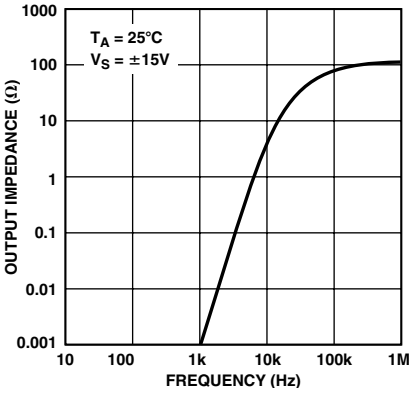
TPC 18. Maximum Output Swing vs. Frequency



TPC 19. Open Loop Gain, Phase vs. Frequency



TPC 20. Small-Signal Overshoot vs. Load Capacitance



TPC 21. Open Loop Output Impedance vs Frequency

APPLICATIONS INFORMATION

Extremely low bias current over a wide temperature range makes the OP297 attractive for use in sample-and-hold amplifiers, peak detectors, and log amplifiers that must operate over a wide temperature range. Balancing input resistances is unnecessary with the OP297. Offset voltage and TCV_{OS} are degraded only minimally by high source resistance, even when unbalanced.

The input pins of the OP297 are protected against large differential voltage by back-to-back diodes and current-limiting resistors. Common-mode voltages at the inputs are not restricted and may vary over the full range of the supply voltages used.

The OP297 requires very little operating headroom about the supply rails and is specified for operation with supplies as low as 2 V. Typically, the common-mode range extends to within 1 V of either rail. The output typically swings to within 1 V of the rails when using a 10 kΩ load.

AC PERFORMANCE

The OP297's ac characteristics are highly stable over its full operating temperature range. Unity gain small-signal response is shown in Figure 4. Extremely tolerant of capacitive loading on the output, the OP297 displays excellent response with 1000 pF loads (Figure 5).

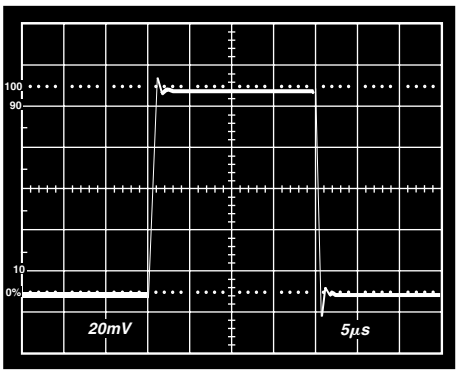


Figure 4. Small-Signal Transient Response (C_{LOAD} = 100 pF, A_{VCL} = 1)

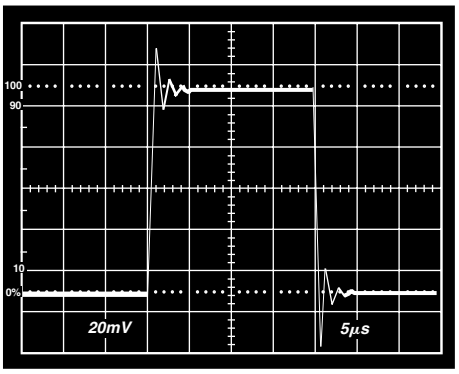


Figure 5. Small-Signal Transient Response (C_{LOAD} = 1000 pF, A_{VCL} = 1)

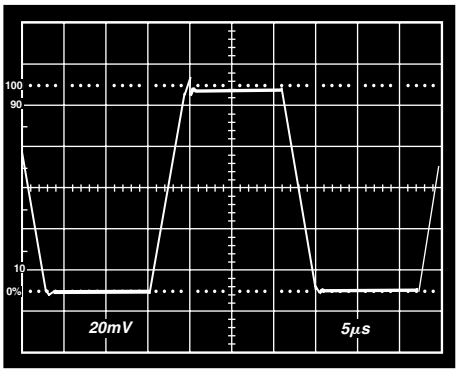


Figure 6. Large-Signal Transient Response (A_{VCL} = 1)

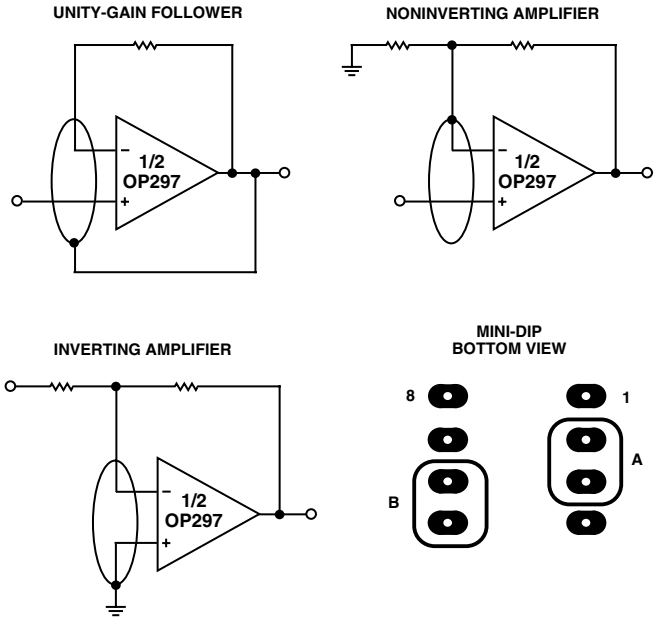


Figure 7. Guard Ring Layout and Connections

GUARDING AND SHIELDING

To maintain the extremely high input impedances of the OP297, care must be taken in circuit board layout and manufacturing. Board surfaces must be kept scrupulously clean and free of moisture. Conformal coating is recommended to provide a humidity barrier. Even a clean PC board can have 100 pA of leakage currents between adjacent traces, so guard rings should be used around the inputs. Guard traces are operated at a voltage close to that on the inputs, as shown in Figure 7, so that leakage currents become minimal. In noninverting applications, the guard ring should be connected to the common-mode voltage at the inverting input. In inverting applications, both inputs remain at ground, so the guard trace should be grounded. Guard traces should be on both sides of the circuit board.

OPEN-LOOP GAIN LINEARITY

The OP297 has both an extremely high gain of 2000 V/mV minimum and constant gain linearity. This enhances the precision of the OP297 and provides for very high accuracy in high closed loop gain applications. Figure 8 illustrates the typical open-loop gain linearity of the OP297 over the military temperature range.

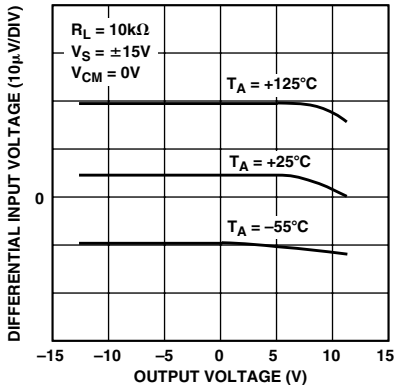


Figure 8. Open-Loop Linearity of the OP297

APPLICATIONS

PRECISION ABSOLUTE VALUE AMPLIFIER

The circuit of Figure 9 is a precision absolute value amplifier with an input impedance of 30 MΩ. The high gain and low TCV_{OS} of the OP297 ensure accurate operation with microvolt input signals. In this circuit, the input always appears as a common-mode signal to the op amps. The CMR of the OP297 exceeds 120 dB, yielding an error of less than 2 ppm.

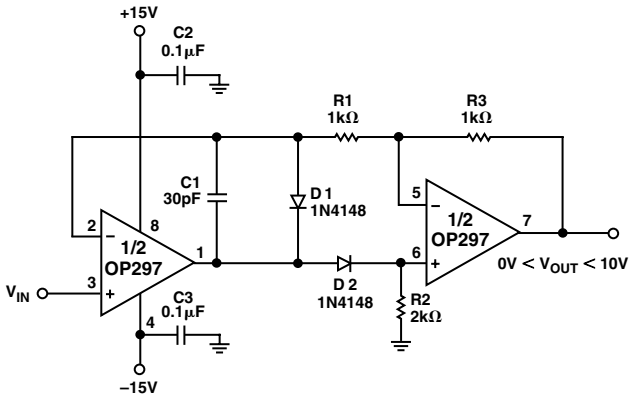


Figure 9. Precision Absolute Value Amplifier

PRECISION CURRENT PUMP

Maximum output current of the precision current pump shown in Figure 10 is ±10 mA. Voltage compliance is ±10 V with ±15 V supplies. Output impedance of the current transmitter exceeds 3 MΩ with linearity better than 16 bits.

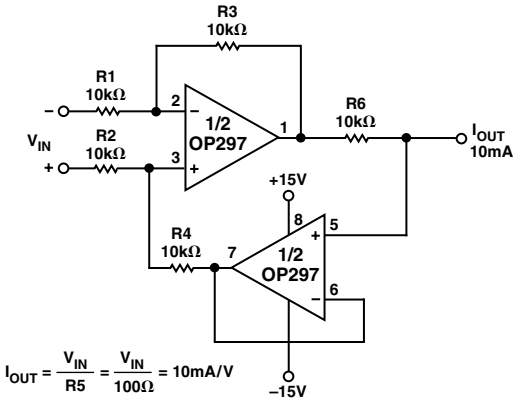


Figure 10. Precision Current Pump

PRECISION POSITIVE PEAK DETECTOR

In Figure 11, the C_H must be of polystyrene, PTFE, or polyethylene to minimize dielectric absorption and leakage. The droop rate is determined by the size of C_H and the bias current of the OP297.

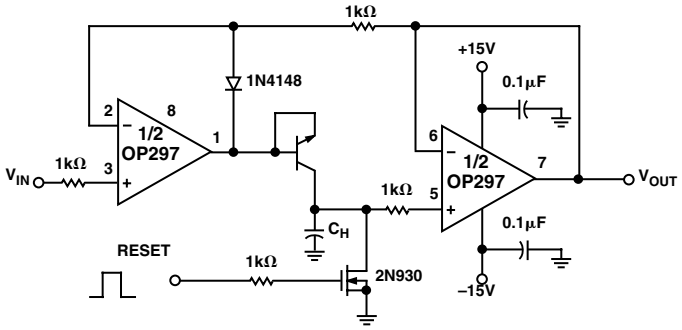


Figure 11. Precision Positive Peak Detector

SIMPLE BRIDGE CONDITIONING AMPLIFIER

Figure 12 shows a simple bridge conditioning amplifier using the OP297. The transfer function is

$$V_{OUT} = V_{REF}\left(\frac{\Delta R}{R + \Delta R}\right)\frac{R_F}{R}$$

The REF43 provides an accurate and stable reference voltage for the bridge. To maintain the highest circuit accuracy, R_F should be 0.1% or better with a low temperature coefficient.

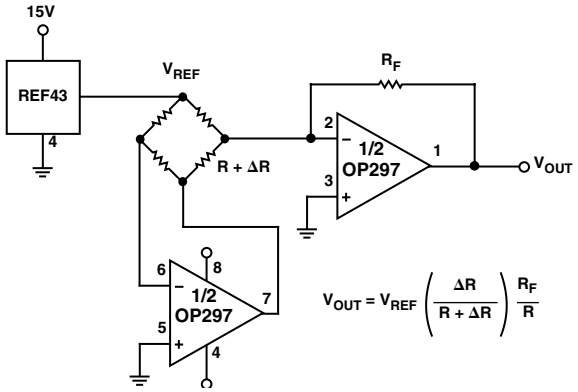


Figure 12. A Simple Bridge Conditioning Amplifier Using the OP297

NONLINEAR CIRCUITS

Due to its low input bias currents, the OP297 is an ideal log amplifier in nonlinear circuits such as the square and square-root circuits shown in Figures 13 and 14. Using the squaring circuit of Figure 13 as an example, the analysis begins by writing a voltage loop equation across transistors Q1, Q2, Q3, and Q4.

$$V_{T1} ln\left(\frac{I_{IN}}{I_{S1}}\right) + V_{T2} ln\left(\frac{I_{IN}}{I_{S2}}\right) = V_{T3} ln\left(\frac{I_O}{I_{S3}}\right) + V_{T4} ln\left(\frac{I_{REF}}{I_{S4}}\right)$$

All the transistors of the MAT04 are precisely matched and at the same temperature, so the I_S and V_T terms cancel, giving

$$2\ ln\ I_{IN} = ln\ I_O + ln\ I_{REF} = ln\left(I_O \times I_{REF}\right)$$

Exponentiating both sides of the equation leads to

$$I_O = \frac{\left(I_{IN}\right)^2}{I_{REF}}$$

Op amp A2 forms a current-to-voltage converter, which gives $V_{OUT} = R2 \times I_O$. Substituting (V_{IN}/R1) for I_{IN} and the above equation for I_O yields

$$V_{OUT} = \left(\frac{R2}{I_{REF}}\right)\left(\frac{V_{IN}}{R1}\right)^2$$

A similar analysis made for the square-root circuit of Figure 14 leads to its transfer function

$$V_{OUT} = R2\sqrt{\frac{\left(V_{IN}\right)\left(I_{REF}\right)}{R1}}$$

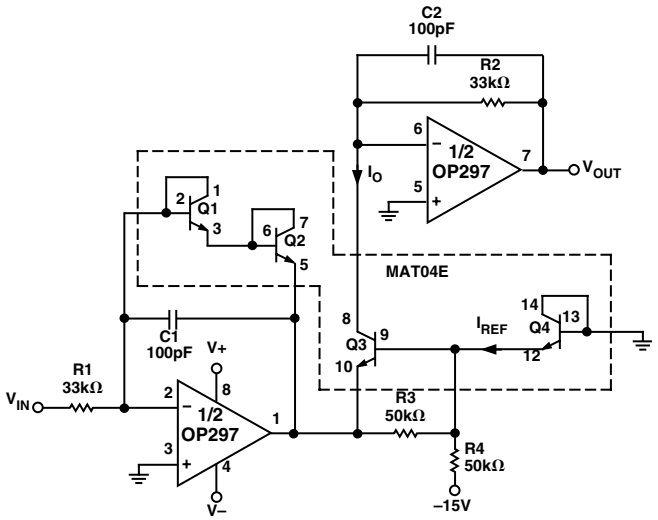


Figure 13. Squaring Amplifier

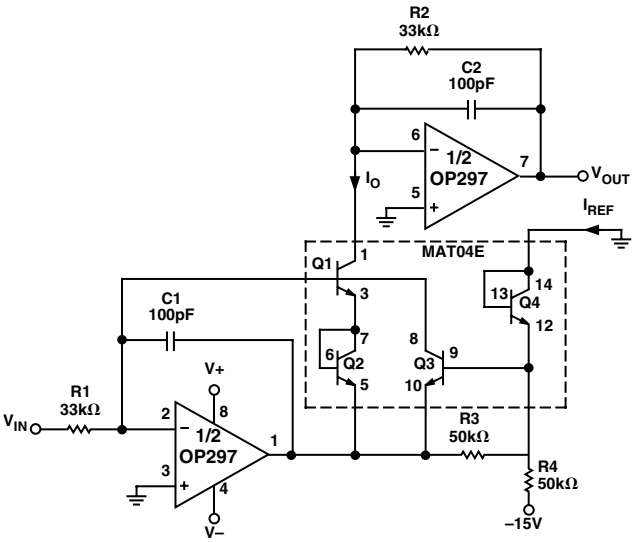


Figure 14. Square-Root Amplifier

In these circuits, I_{REF} is a function of the negative power supply. To maintain accuracy, the negative supply should be well regulated. For applications where very high accuracy is required, a voltage reference may be used to set I_{REF}. An important consideration for the squaring circuit is that a sufficiently large input voltage can force the output beyond the operating range of the output op amp. Resistor R4 can be changed to scale I_{REF}, or R1, and R2 can be varied to keep the output voltage within the usable range.

Unadjusted accuracy of the square-root circuit is better than 0.1% over an input voltage range of 100 mV to 10 V. For a similar input voltage range, the accuracy of the squaring circuit is better than 0.5%.

OP297 SPICE MACRO MODEL

Figures 14 and 15 show the node end net list for a SPICE macro model of the OP297. The model is a simplified version of the actual device and simulates important dc parameters such as V_{OS}, I_{OS}, I_B, A_{VO}, CMR, V_O, and I_{SY}. AC parameters such as slew rate, gain and phase response, and CMR change with frequency are also simulated by the model.

The model uses typical parameters for the OP297. The poles and zeros in the model were determined from the actual open- and closed-loop gain and phase response of the OP297. In this way, the model presents an accurate ac representation of the actual device. The model assumes an ambient temperature of 25°C.

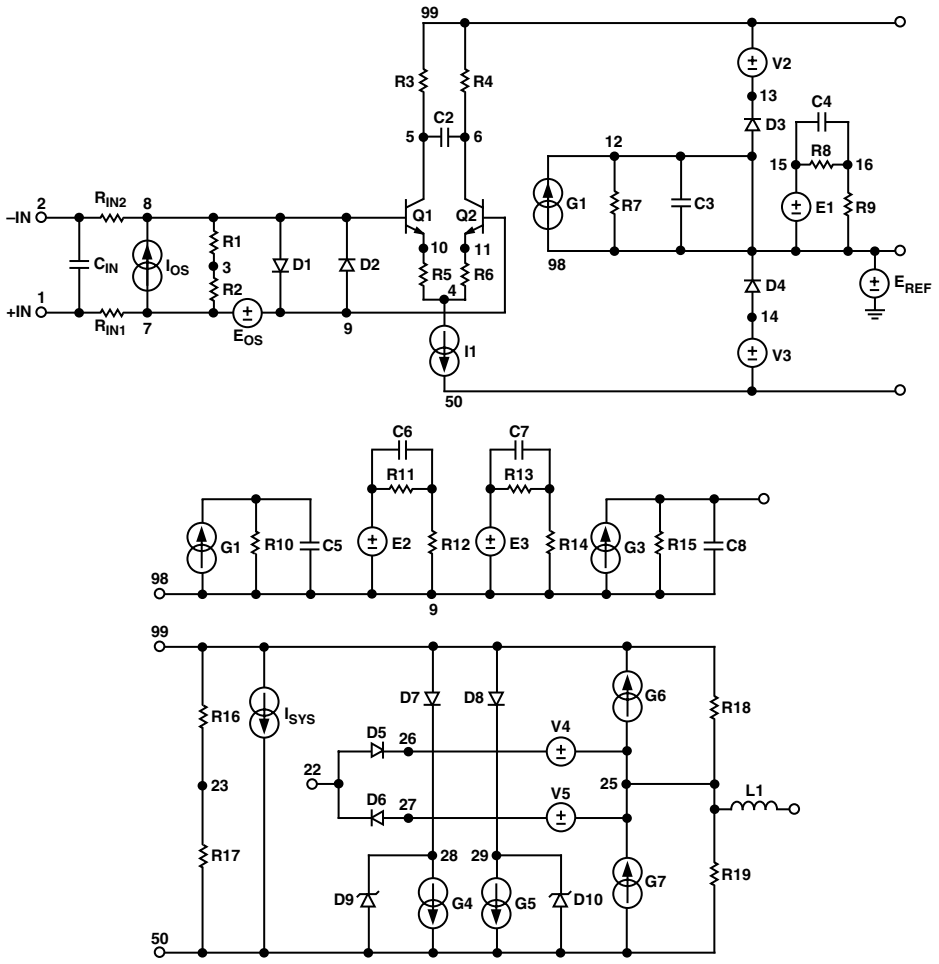


Figure 15. Macro Model

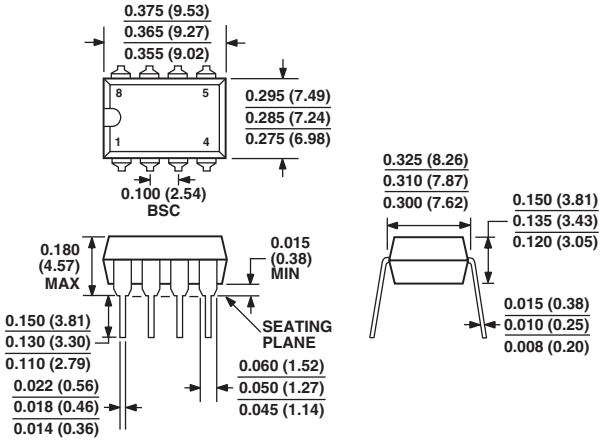
SPICE Net List

```
*OP297 SPICE MACRO-MODEL
*
*NODE ASSIGNMENTS
                          NONINVERTING INPUT
                          |   INVERTING INPUT
                          |   |   OUTPUT
                          |   |   |   POSITIVE SUPPLY
                          |   |   |   |   NEGATIVE SUPPLY
                          |   |   |   |   |
*SUBCKT OP297             1   2   30  99  50
*
*INPUT STAGE & POLE AT 6 MHz
*
RIN1    1       7       2500
RIN2    2       8       2500
R1      8       3       5E11
R2      7       3       5E11
R3      5       99      612
R4      6       99      612
CIN     7       8       3E-12
C2      5       6       21.67E-12
I1      4       50      0.1E-3
IOS     7       8       20E-12
EOS     9       7       POLY(1)  19 23 25E-6 1
Q1      5       8       10       QX
Q2      6       9       11       QX
R5      10      4       96
R6      11      4       96
D1      8       9       DX
D2      9       8       DX
*
EREF    98      0       23 0 1
*
*GAIN STAGE & DOMINANT POLE AT 0.13 HZ
*
R7      12      98      2.45E9
C3      12      98      500E-12
G1      98      12      5 6      1.634E-3
V2      99      13      1.5
V3      14      50      1.5
D3      12      13      DX
D4      14      12      DX
*
*NEGATIVE ZERO AT -1.8 MHz
*
R8      15      16      1E6
C4      15      16      –88.4E-15
R9      16      98      1
E1      15      98      12 23 1E6
*
*POLE AT 1.8 MHz
*
R10     17      98      1E6
C5      17      98      88 4E-15
G2      98      17      16 23 1 E-6
*
*COMMON-MODE GAIN NETWORK WITH ZERO AT 50 HZ
*
R11     18      19      1E6
C6      18      19      3.183E-9
R12     19      98      1
E2      18      98      3 23 100E-3
*
*POLE AT 6 MHz
*
R15     22      98      1E6
C8      22      98      26.53E-15
G3      98      22      17 23 1 E-6
*
*OUTPUT STAGE
*
R16     23      99      160E3
R17     23      50      160E3
ISY     99      50      331E-6
R18     25      99      200
R19     25      50      200
L1      25      30      1E-7
G4      28      50      22 25 5E-3
G5      29      50      25 22 5E-3
G6      25      99      99 22 5E-3
G7      50      25      22 50 5E-3
V4      26      25      1.8
V5      25      27      1.3
D5      22      26      DX
D6      27      22      DX
D7      99      28      DX
D8      99      29      DX
D9      50      28      DY
D10     50      29      DY
*
*MODELS USED
*
.MODEL QX NPN BF=2.5E6)
.MODEL DX D IS = 1E-15)
.MODEL DY D IS = 1E-15 BV = 50)
.ENDS OP297
```

OUTLINE DIMENSIONS

8-Lead Plastic Dual In-Line Package [PDIP]
P-Suffix
(N-8)

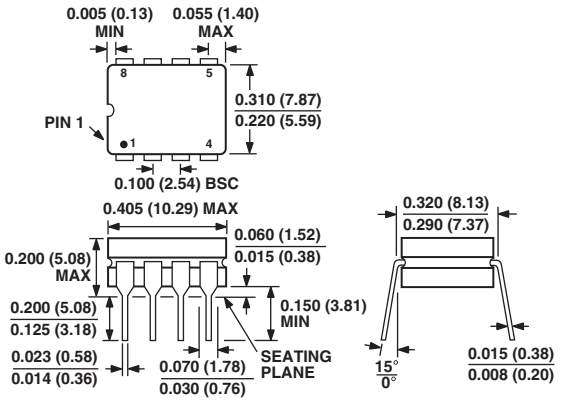
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Ceramic Dual In-Line Package [CERDIP]
Z-Suffix
(Q-8)

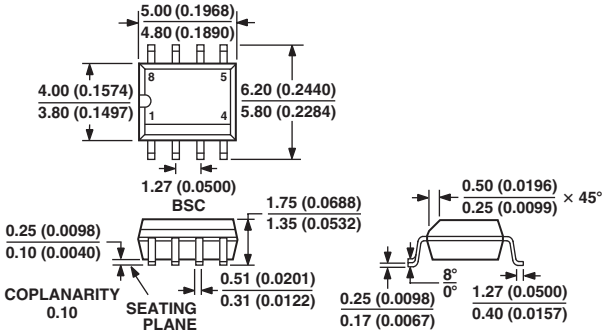
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Standard Small Outline Package (SOIC)
Narrow Body
S-Suffix
(R-8)

Dimensions shown in millimeters and (inches)



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Revision History

Location	Page
7/03—Data Sheet changed from REV. D to REV. E.	
Changes to TPCS 13 and 16	4
Edits to Figures 12 and 14	8
Changes to NONLINEAR CIRCUITS Section	8
10/02—Data Sheet changed from REV. C to REV. D.	
Edits to Figure 16	6
10/02—Data Sheet changed from REV. B to REV. C.	
Edits to SPECIFICATIONS	2
Deleted WAFER TEST LIMITS	3
Deleted DICE CHARACTERISTICS	3
Deleted ABSOLUTE MAXIMUM RATINGS	4
Edits to ORDERING GUIDE	4
Updated OUTLINE DIMENSIONS	12

C00300–0–7/03(E)