

NTE66 MOSFET N–Ch, Enhancement Mode High Speed Switch

Description:

The NTE66 is a TMOS Power FET in a TO220 type package designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

Features:

- Lower $R_{DS(ON)}$
- Improved Inductive Ruggedness
- Fast Switching Times
- Lower Input Capacitance
- Extended Safe Operating Area
- Improved High Temperature Reliability

Absolute Maximum Ratings:

Drain–Source Voltage ($T_J = +25^{\circ}\text{C}$ to $+150^{\circ}\text{C}$), V_{DSS}	100V
Drain–Gate Voltage ($R_{GS} = 1\text{M}\Omega$, $T_J = +25^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), V_{DGR}	100V
Gate–Source Voltage, V_{GS}	$\pm 20\text{V}$
Continuous Drain Current, I_D	
$T_C = +25^{\circ}\text{C}$	14A
$T_C = +100^{\circ}\text{C}$	10A
Pulsed Drain Current (Note 2), I_{DM}	56A
Pulsed Gate Current, I_{GM}	$\pm 1.5\text{A}$
Single Pulsed Avalanche Energy (Note 3), E_{AS}	69mJ
Avalanche Current, I_{AS}	14A
Total Power Dissipation ($T_C = +25^{\circ}\text{C}$), P_D	77W
Derate Above 25°C	0.62W/ $^{\circ}\text{C}$
Operating Junction Temperature Range, T_J	-55° to $+150^{\circ}\text{C}$
Storage Temperature Range, T_{stg}	-55° to $+150^{\circ}\text{C}$
Lead Temperature (During Soldering, 1/8" from case, 5sec max.), T_L	$+300^{\circ}\text{C}$
Thermal Resistance, Junction–to–Case, $R_{\theta JC}$	1.62K/W
Thermal Resistance, Junction–to–Ambient, $R_{\theta JA}$	80K/W
Thermal Resistance, Case–to–Sink (Mounting surface flat, smooth, and greased), $R_{\theta CS}$	0.5K/W

Note 1. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

Note 2. Repetitive rating: Pulse width limited by max, junction temperature.

Note 3. $L = 0.53\text{mH}$, $V_{dd} = 25\text{V}$, $R_G = 25\Omega$, Starting $T_J = +25^{\circ}\text{C}$.

Electrical Characteristics: ($T_C = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain–Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	100	–	–	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	–	4.0	V
Gate–Source Leakage, Forward	I_{GSS}	$V_{GS} = 20V$	–	–	100	nA
Gate–Source Leakage, Reverse	I_{GSS}	$V_{GS} = -20V$	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Max. Rating}, V_{GS} = 0V$	–	–	250	μA
		$V_{DS} = \text{Max. Rating} \times 0.8, V_{GS} = 0V, T_C = +125^\circ\text{C}$	–	–	1000	μA
On–State Drain–Source Current	$I_{D(on)}$	$V_{DS} > I_{D(on)} \times R_{DS(on)} \text{max}, V_{GS} = 10V, \text{Note 1}$	14	–	–	A
Static Drain–Source On–State Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 8.3A, \text{Note 1}$	–	0.10	0.16	Ω
Forward Transconductance	g_{fs}	$V_{DS} \geq 50V, I_D = 8.3A, \text{Note 1}$	5.1	7.6	–	mhos
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 25V, f = 1\text{MHz}$	–	640	–	pF
Output Capacitance	C_{oss}		–	240	–	pF
Reverse Transfer Capacitance	C_{rss}		–	72	–	pF
Turn–On Delay Time	$t_{d(on)}$	$V_{DD} = 0.5BV_{DSS}, I_D = 8.3A, Z_O = 12\Omega$ (MOSFET switching times are essentially independent of operating temperature)	–	10	15	ns
Rise Time	t_r		–	34	51	ns
Turn–Off Delay Time	$t_{d(off)}$		–	23	35	ns
Fall Time	t_f		–	24	36	ns
Total Gate Charge (Gate–Source Plus Gate–Drain)	Q_g	$V_{GS} = 10V, I_D = 14A, V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)	–	17	26	nC
Gate–Source Charge	Q_{gs}		–	3.7	5.5	nC
Gate–Drain (“Miller”) Charge	Q_{gd}		–	7	11	nC

Note 1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

Source–Drain Diode Ratings and Characteristics:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Continuous Source Current (Body Diode)	I_S		–	–	14	A
Pulse Source Current (Body Diode)	I_{SM}	Note 2	–	–	56	A
Diode Forward Voltage	V_{SD}	$T_C = +25^\circ\text{C}, I_S = 14A, V_{GS} = 0V$	–	–	2.5	V
Reverse Recovery Time	t_{rr}	$T_J = +25^\circ\text{C}, I_F = 14A, dI_F/dt = 100A/\mu s$	–	120	250	ns

Note 1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

Note 2. Repetitive rating: Pulse width limited by max. junction temperature.

