High-Current Complementary Silicon Transistors

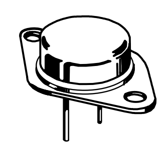
. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain —
  h_{FE} = 1000 (Min) @ I_C – 20 Adc
- Monolithic Construction with Built–in Base Emitter Shunt Resistor
- Junction Temperature to +200°C

PNP
MJ11015
NPN
MJ11012
MJ11016*

*ON Semiconductor Preferred Device

30 AMPERE DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON 60–120 VOLTS 200 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ11012	MJ11015 MJ11016	Unit
Collector–Emitter Voltage	V_{CEO}	60	120	Vdc
Collector–Base Voltage	V_{CB}	60	120	Vdc
Emitter–Base Voltage	V_{EB}	5		Vdc
Collector Current	I_C	30		Adc
Base Current	I_B	1		Adc
Total Device Dissipation @T_C = 25°C Derate above 25°C @ T_C = 100°C	P_D	200 1.15		Watts W/°C
Operating Storage Junction Temperature Range	T_J, T_{stg}	–55 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.87	°C/W
Maximum Lead Temperature for Soldering Purposes for ≤ 10 Seconds.	T_L	275	°C

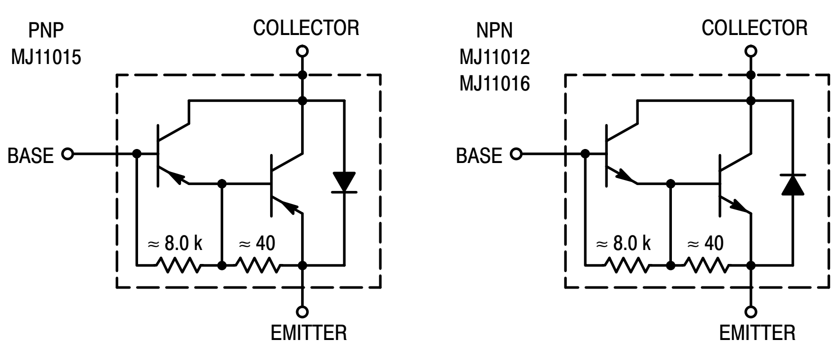


Figure 1. Darlington Circuit Schematic

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

May, 2001 – Rev. 4
Publication Order Number:
MJ11012/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristics		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage(1) (I_C = 100 mAdc, I_B = 0)	MJ11012	$V_{(BR)CEO}$	60	—	Vdc
	MJ11015, MJ11016		120	—	
Collector–Emitter Leakage Current (V_{CE} = 60 Vdc, R_{BE} = 1k ohm)	MJ11012	I_{CER}	—	1	mAdc
(V_{CE} = 120 Vdc, R_{BE} = 1k ohm)	MJ11015, MJ11016		—	1	
(V_{CE} = 60 Vdc, R_{BE} = 1k ohm, T_C = 150°C)	MJ11012		—	5	
(V_{CE} = 120 Vdc, R_{BE} = 1k ohm, T_C = 150°C)	MJ11015, MJ11016		—	5	
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	5	mAdc
Collector–Emitter Leakage Current (V_{CE} = 50 Vdc, I_B = 0)		I_{CEO}	—	1	mAdc
ON CHARACTERISTICS(1)					
DC Current Gain (I_C = 20 Adc,V_{CE} = 5 Vdc)		h_{FE}	1000	—	—
(I_C = 30 Adc, V_{CE} = 5 Vdc)			200	—	
Collector–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 200 mAdc)		$V_{CE(sat)}$	—	3	Vdc
(I_C = 30 Adc, I_B = 300 mAdc)			—	4	
Base–Emitter Saturation Voltage (I_C = 20 A, I_B = 200 mAdc)		$V_{BE(sat)}$	—	3.5	Vdc
(I_C = 30 A, I_B = 300 mAdc)			—	5	
DYNAMIC CHARACTERISTICS					
Current–Gain Bandwidth Product (I_C = 10 A, V_{CE} = 3 Vdc, f = 1 MHz)		h_{fe}	4	—	MHz

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

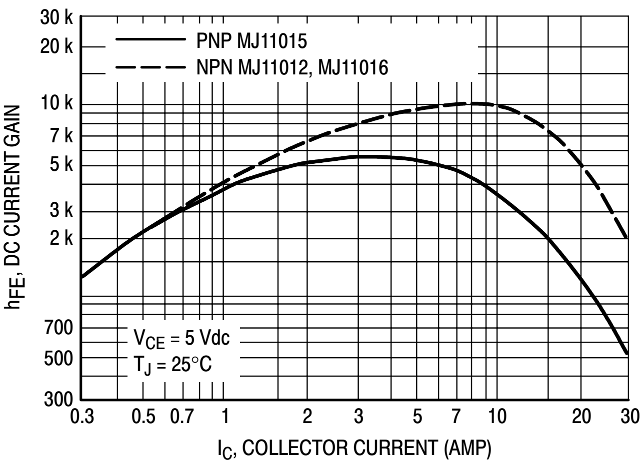


Figure 2. DC Current Gain (1)

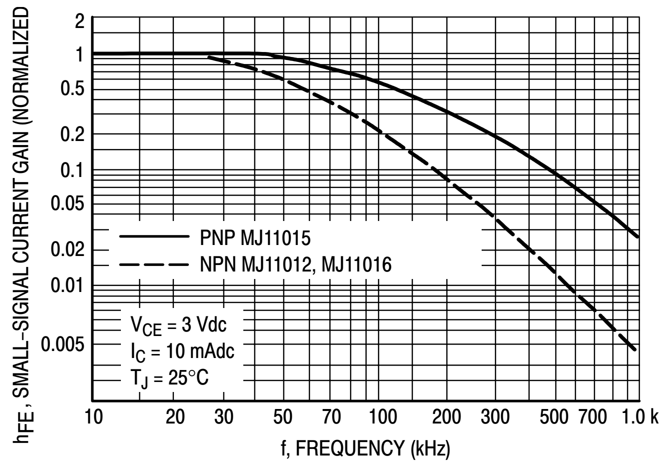


Figure 3. Small–Signal Current Gain

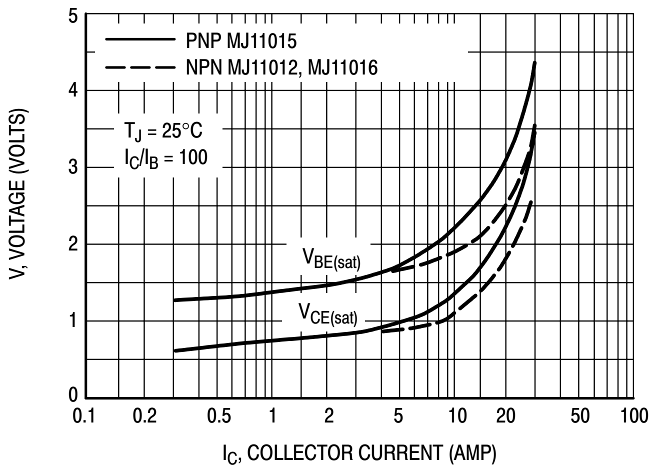


Figure 4. "On" Voltages (1)

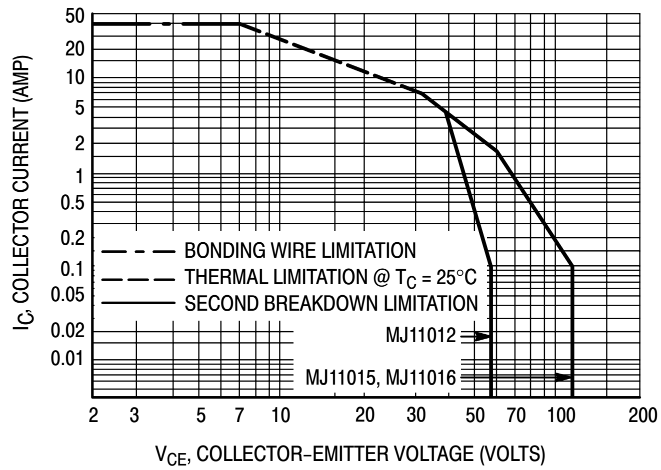


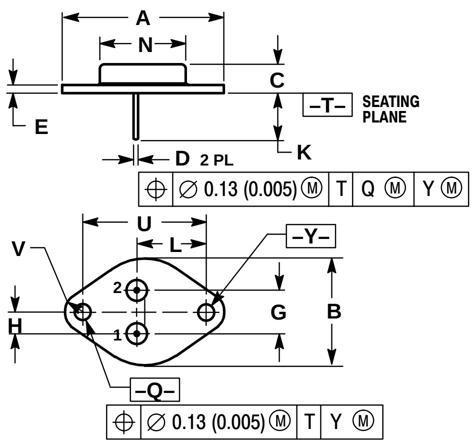
Figure 5. Active Region DC Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and secondary breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operations e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

PACKAGE DIMENSIONS

CASE 1–07
TO–204AA (TO–3)
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

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CASE: COLLECTOR

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