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MAP3201

High current switch mode PWM LED Driver

MAP3201 – High current switch mode PWM LED Driver

General Description

The MAP3201 is a high efficiency current mode PWM driver. It is designed for LED driver that is used as the light source of LCD panel. The controller can achieve efficiency higher than 90% for buck and boost applications.

The MAP3201 for accurate LED dimming control use external PWMI signal and set internal frequency by external resistor which is programmable.

The MAP3201 has a stable operation with wide input voltage because it can be operated as separated V_{CC} with input voltage It has a auto-restart recovery protection if the system occur fault signal. it can provide a good safety features.

Multiple MAP3201 have synchronized to each others or to other external clock which is generated by Sync Pin.

The MAP3201 provide a 0.4A source current and 0.8A Sink current gate driver. This can be suitable for high power application. Using BCD process, the MAP3201 has a good immunity at switching noise.

The MAP3201' application can be so easy to making lowest cost system.

The MAP3201 is available in 16-Lead SOIC package and it is offered in Halogen-free (fully RoHS compliant).
For more information, please contact local MagnaChip sales office in world-wide or visit MagnaChip's website at *www.magnachip.com*.

Features

- PWM Interface LED Driver
- Current Mode Control Type
- Auto Restart Mode Protection
- Output Over Voltage Protection
- Programmable LED Short Current Protection
- Power Supply V_{CC}=12V (Max 20V)
- Programmable LED Current Set (FBP)
- Programmable Boost switch current limit
- Synchronization to peer-to-peer or   external clock
- Fully RoHS Compliant

Application

RGB and White LED Backlighting applications
General LED lighting applications

Typical Application Circuit

MAP3201 – High current switch mode PWM LED Driver
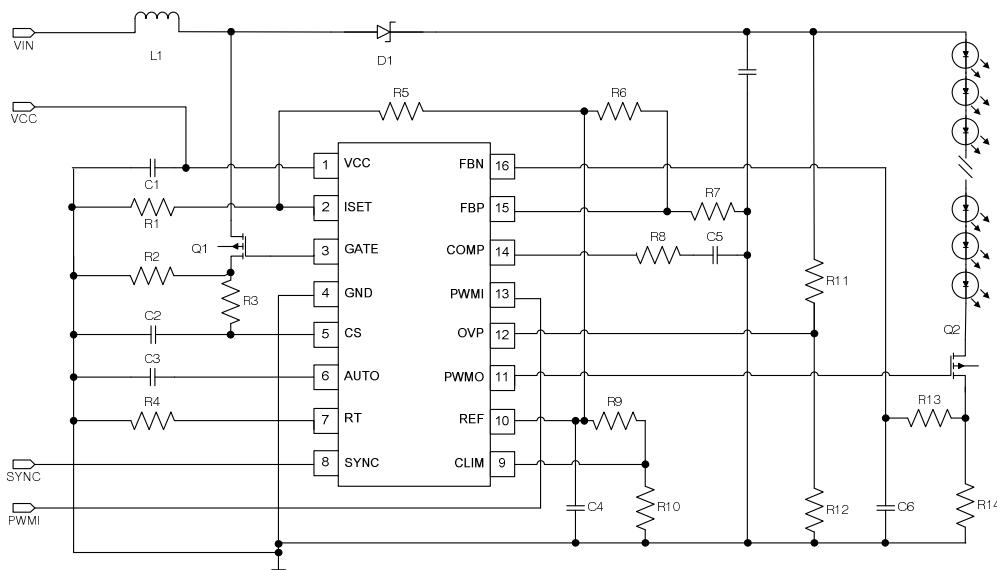
Ordering Information

Part Number	Part Marking	Junction Temperature Range	Package	RoHS Status
MAP3201SIH	SELC2010M	-40℃ to +125℃	16 Leads SOIC	Halogen Free

Absolute Maximum Ratings

PARAMETER	VALUE	UNIT
VCC	-0.3 ~ 20	V
GATE, PWMO	-0.3 ~ 20	V
AUTO,CS, ISET,RT,SYNC,CLIM,REF,OVP,PWMI,COMP,FBP,FBN	-0.3 ~ 5	V
Operating Junction Temperature Range	-40 ~ 125	℃
Storage Temperature Range	-65 ~ 150	℃
Lead temperature(soldering, 10sec)	260	℃
Thermal Resistance (θJA)	105	℃/W

Electrical Characteristics

Vcc=12V, VPWMI=5V, CGATE=CPWMO=1nF, Ta=25℃, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY						
$V_{CC,OP}$	Input voltage range	Ta=-40℃ ~ 85℃	8.5		18	V
I_Q	Operation quiescent current	PWMI =0V	-	1.2	2	mA
V_{UVLO_R}	Under-voltage lockout threshold	VCC rising	7.5	8	8.5	V
V_{UVLO_F}	Under-voltage lockout hysteresis	VCC falling	-	1	-	V
REFERENCE						
V_{REF}	Reference pin voltage	Ta=-40℃ ~ 85℃	4.90	5.00	5.10	V
		Ta=25℃	4.95	5.00	5.05	V
V_{REFLI}	Line regulation	IREF=0uA, VPWMI=0V, CREF=0.1uF	-	-	0.02	%/V
V_{REFLO}	Load regulation	IREF=0~500uA, VREF=0V, CREF=0.1uF	-	-	1	%/mA
GATE						
I_{SOUR}	Gate short circuit current	VGATE=0, Vcc =12V	0.4	-	-	A
I_{SINK}	Gate sink current	VGATE=12V, Vcc =12V	0.8	-	-	A
T_{RISE}	GATE output rise time	CGATE=1nF, Vcc=12V	-	50	85	ns
T_{FALL}	GATE output fall time	CGATE=1nF, Vcc =12V	-	25	45	ns
Current Sense						
T_{BLANK}	Leading Edge Blanking		100	-	375	ns
T_{DELAY1}	Delay to output of CS comparator(2)	VCOMP=5V, VCLIM=5V, VCS=0V to 600mV step		-	180	ns
T_{DELAY2}	Delay to output of CLIMT comparator(2)	VCOMP =5V, CLIM=300mV, VCS=0V to 400mV step	-	-	180	ns
Internal Transconductance Opamp						
A_V	Open loop DC Gain(2)	-	-	50	-	dB
V_{CM}	Input common-mode range		-0.3	-	3	V
V_O	Output Voltage range	VCC=12V	0.6	-	2.75	V
gm	Transconductance(2)		400	670	1000	uA/V
V_{OFFSET}	Input offset voltage		-5	-	5	mV
I_{BIAS}	Input Bias current		-	0.5	1	nA

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Electrical Characteristics (Continued)

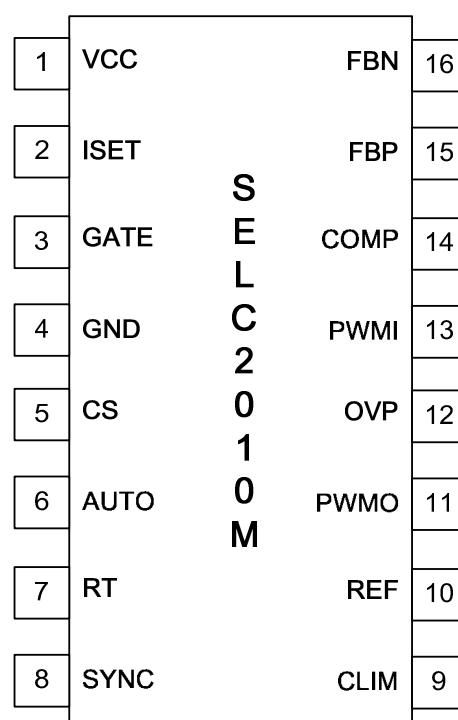V$_{CC}$=12V, V$_{PWMI}$=5V, C$_{GATE}$=C$_{PWMO}$=1nF, Ta=25℃, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Oscillator						
F$_{OSC}$	Oscillator frequency (100KHz ~ 400KHz)	Ta=25℃, RT=500kΩ	95	100	105	kHz
		Ta=–40℃ ~ 85℃, RT=500kΩ	90	100	110	kHz
		Ta=–40℃ ~ 85℃, RT=110kΩ	340	400	460	kHz
D$_{MAX}$	Maximum duty cycle		-	90	-	%
Synchronizing (External Input)						
V$_{IL\_SYNC}$	SYNC Input voltage Low level	-		-	0.8	V
V$_{IH\_SYNC}$	SYNC Input voltage high level	-	2.0	-	-	V
T$_{SYNC\_MIN}$	SYNC minimum input pulse width	VSYNC = 0V to 5V	20	-	-	ns
T$_{SYNC\_MAX}$	SYNC maximum input pulse width	VSYNC = 0V to 5V	-	-	0.05 /F$_{OSC}$	ns
PWM Input						
V$_{PWMI(LO)}$	PWMI input Low voltage	-	-	-	0.8	V
V$_{PWMI(HI)}$	PWMI input High voltage	-	2.0	-		V
R$_{PWMI}$	PWMI pull-down resistance	VPWMI=5V	50	100	150	kΩ
PWM Output						
T$_{RISE,PWMO}$	PWM Output rise time	1nF capacitance at PWMO	-	-	300	ns
T$_{FALL,PWMO}$	PWM Output fall time	1nF capacitance at PWMO		-	200	ns
Auto Restart Protection (AUTO)						
I$_{SO,AUTO}$	Current source at AUTO Pin	-	3	5	8	uA
V$_{TH(H)}$	High threshold at AUTO Pin	-	2.7	3	3.3	V
V$_{TH(L)}$	Low threshold at AUTO Pin	-	0.9	1	1.1	V
Over Voltage Protection (OVP)						
V$_{OVP}$	Over voltage protection		2.94	3.0	3.06	V
V$_{OVPH}$	Over voltage protection hysteresis	-	-	0.3	-	V
T$_{OVP}$	OVP Filtering time(2)		-	200	-	ns

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Electrical Characteristics (Continued)

MAP3201 – High current switch mode PWM LED Driver

V_{CC}=12V, V_{PWMI}=5V, C_{GATE}=C_{PWMO}=1nF, Ta=25℃, unless otherwise specified

Programmable Short current protection (ISET)						
$V_{CM,ISET}$	Input common-mode range of comparator	-	-0.3	-	3	V
$V_{OFF,ISET}$	Input offset voltage of comparator	V_{ISET}=1V	-20	-	20	mV
T_{OFF}	Propagation time for short current detection (2)	V_{ISET}=1V, V_{FBN}=0.9 to 1.1V step V_{PWMO} goes from high to low	-	-	250	ns

Note 1: Stress beyond the maximum ratings listed above may incur permanent damage to the device. Operating above the recommended conditions for extended time may stress the device and affect device reliability. Also the device may not operate normally above the recommended operating conditions. These are stress ratings only.
Note 2: These parameters, although guaranteed by design, are not tested in mass productioin.

MAP3201 – High current switch mode PWM LED Driver

Pin Description

PIN NO		Description
1	VCC	Power Supply Input
2	ISET	Programmable Short Current Protection Set
3	GATE	Gate drive Output for Boost Convert
4	GND	GND
5	CS	Current sense of the Boost Convert
6	AUTO	Auto Restart mode control for protection
7	RT	Oscillator frequency set of the Boost Converter
8	SYNC	Oscillators to lock to the highest frequency
9	CLIM	Programmable Boost Input current limit
10	REF	Reference voltage
11	PWMO	PWM Gate Driver Output
12	OVP	Over voltage protection
13	PWMI	PWM Gate Driver Input
14	COMP	Error Amp. Compensation
15	FBP	Error Amp. Non-inverting Input/Positive Current Sense
16	FBN	Error Amp. Inverting Input/Negative Current Sense

1	VCC	FBN	16
2	ISET	FBP	15
3	GATE	COMP	14
4	GND	PWMI	13
5	CS	OVP	12
6	AUTO	PWMO	11
7	RT	REF	10
8	SYNC	CLIM	9

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Functional Block Diagram
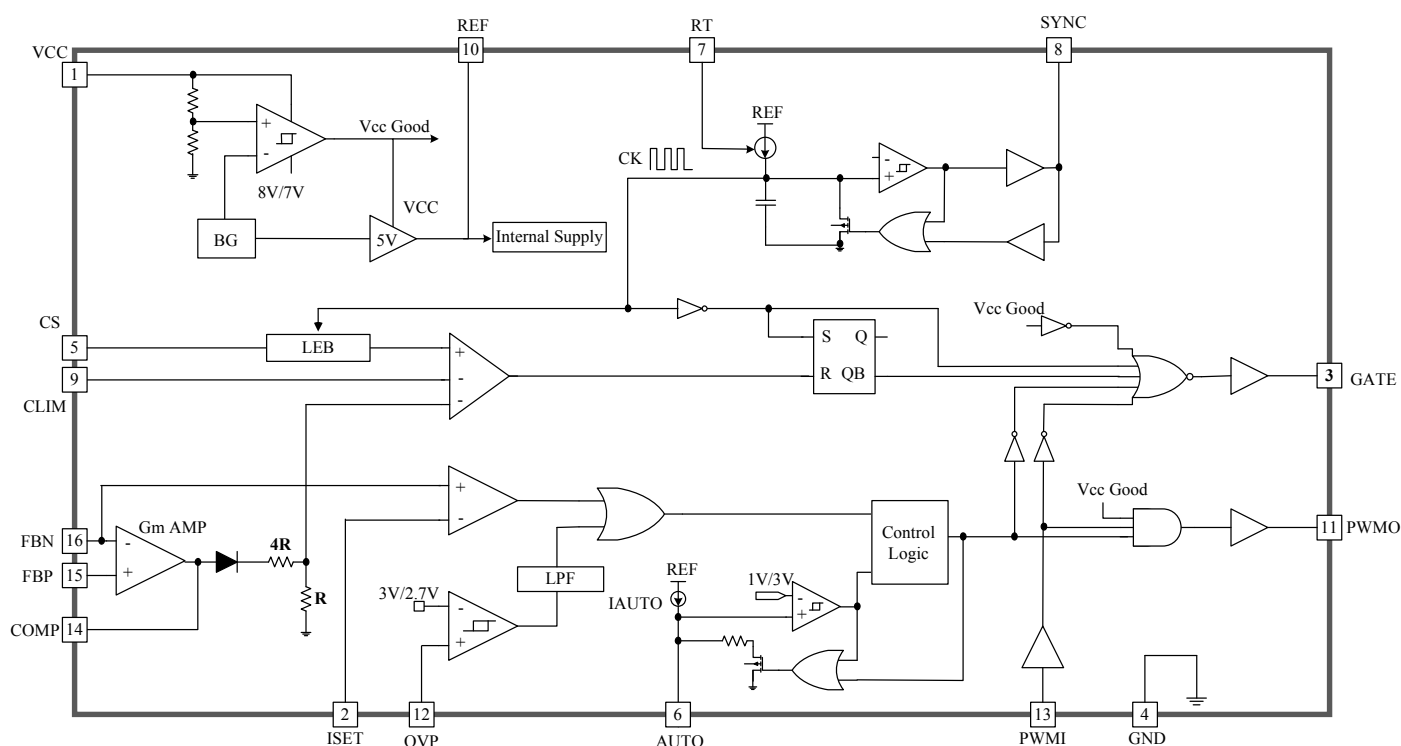
Physical Dimensions

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No	REVISION ITEM		DATE	NAME

Symbol	Min	Nom	Max
A	-	-	1.80
A1	0.05	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
b1	0.28	-	0.48
C	0.10	-	0.30
c1	0.10	-	0.23
D	9.70	-	10.10
E	5.70	-	6.30
E1	3.75	-	4.15
e	1.14	1.27	1.40
L	0.40	-	1.27
L1	1.04 REF		
L2	0.25 BSC		
R	0.07	-	-
R1	0.07	-	-
θ	0°	-	8°
θ1	0°	-	15°

DIV'D	NAME	DATE	TITLE	16 SOP PACKAGE DRAWING
DES.BY	Karl Lee	'09.11.19	DWG.NO	MBKD–D0786
CH.BY				
APR.BY			REV.NO	0	SHEET	1/1
SCALE	NA	UNIT	mm	
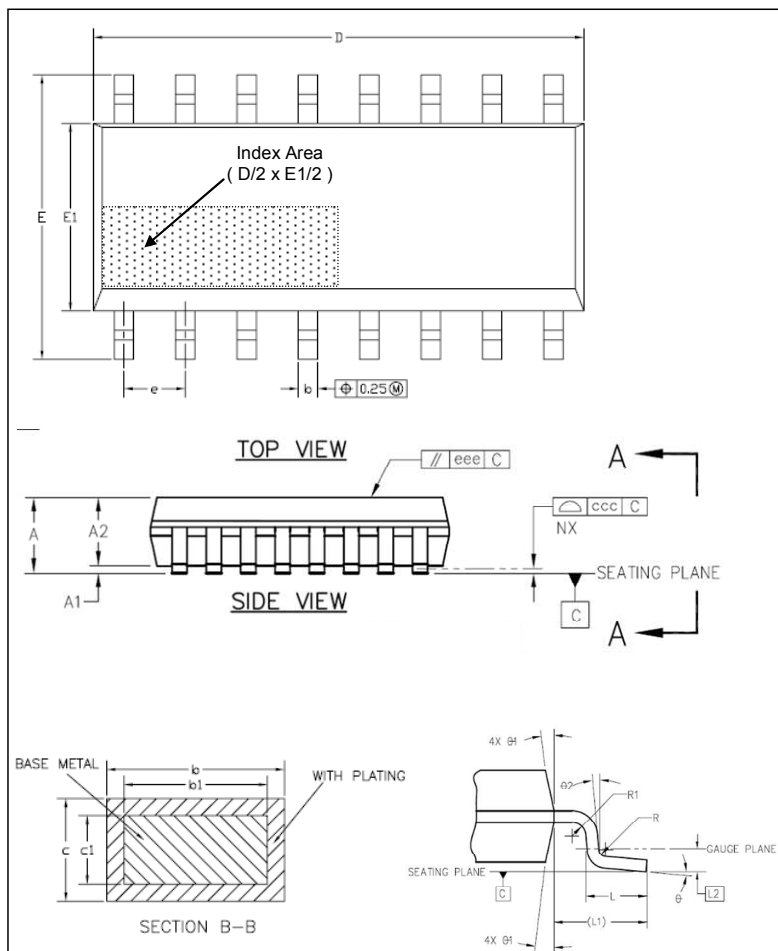
Reference JEDEC No. MS-012 (AC)

Typical Operating Characteristics

The following conditions apply: VCC =12V, RRT = 500 kΩ, VPWMI = 5V

MAP3201 – High current switch mode PWM LED Driver

Quiescent Current vs. Vcc
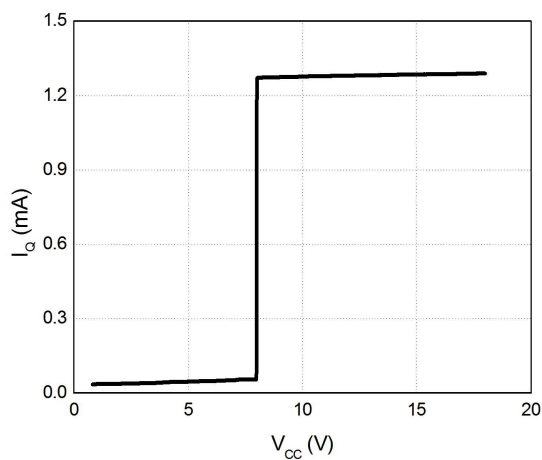
Quiescent Current vs. TEMP.
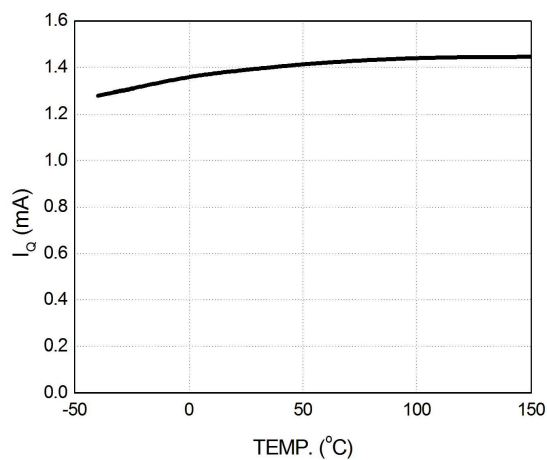
VREF vs. TEMP.
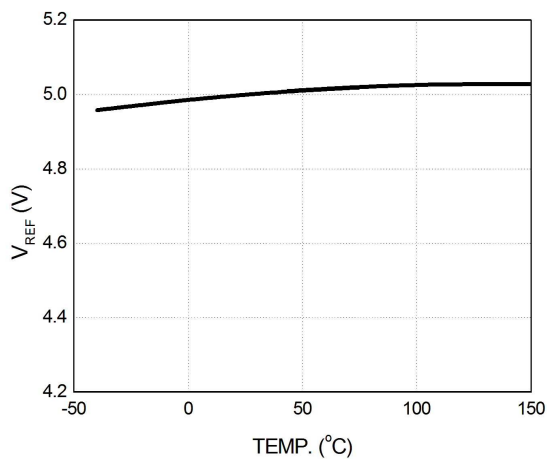
VREF Load Regulation Voltage
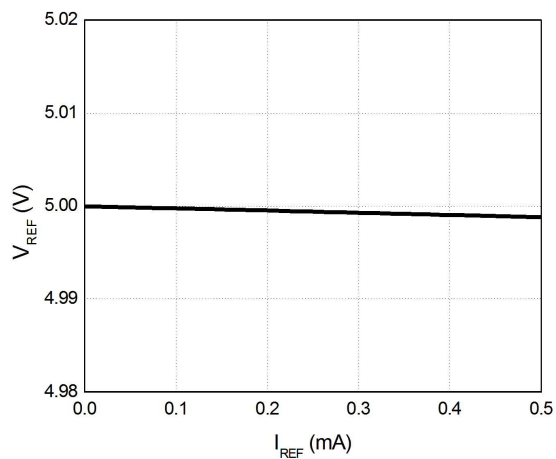
VREF Line Regulation Voltage
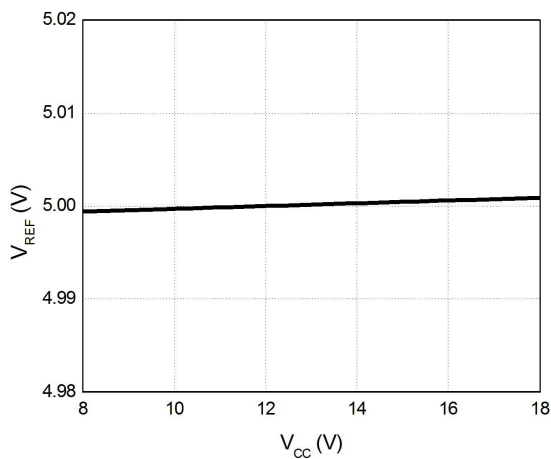
Under Voltage Lock Out
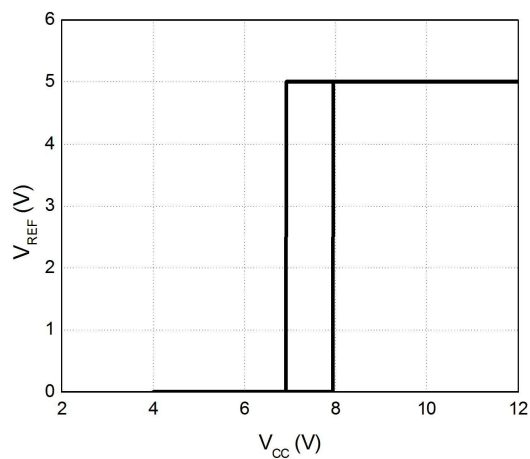
MAP3201 – High current switch mode PWM LED Driver

Typical Operating Characteristics

The following conditions apply: VCC =12V, RRT = 500 kΩ, VPWMI = 5V

Over Voltage Protection

Frequency vs. RT

MAP3201 – High current switch mode PWM LED Driver
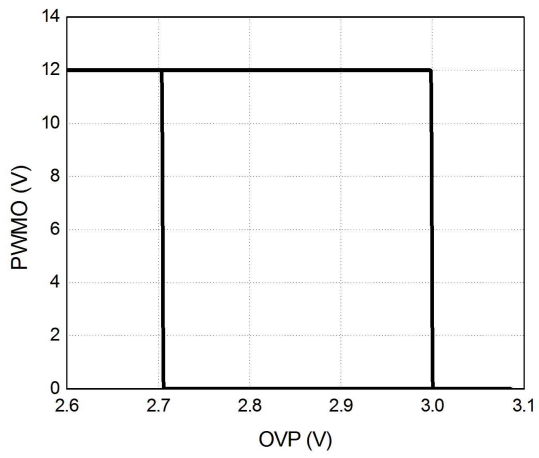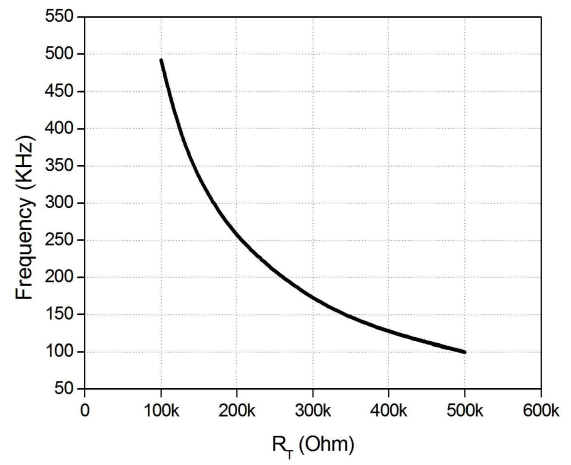
Current Mode Boost switching regulator operation

The MAP 3201 is operated in current mode PWM Boost regulation method, which shows fast frequency response while maintaining stable output voltage.

It features stable response by using the recommended combination of resistor and capacitor at COMP and GND pin for specific condition of wide input voltage, Output voltage and variable Load condition.

Internal 5V Low Dropout Regulator

The MAP3201 has LDO embedded in it to supply Internal analog, logic circuit and external REF Pin. This LDO operates at a voltage level where Vcc is higher than the UVLO voltage. It provides maximum 10mA of output current through regulator which has 2% accuracy of performance.

To stabilize the voltage of REF Pin, it is recommended to use low ESR capacitor which is as low as 1uF and connect it between REF and GND Pin, and install it as close as to Pin.

Boost Converter Switching Frequency

The MAP3201 can set the switching frequency of Boost converter by connecting external resistor between RT and GND Pin. Recommended switching frequency is 100 KHz to 400 KHz.
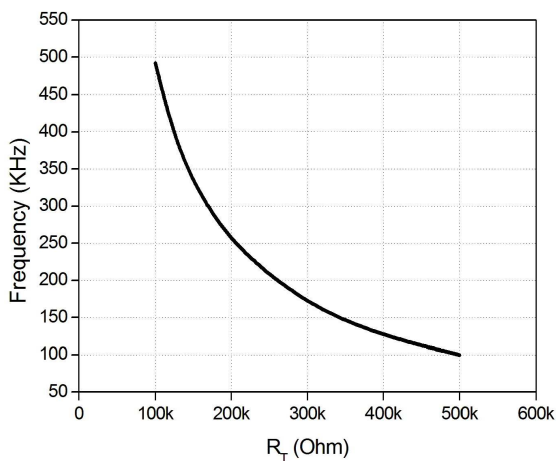See Figure 1 for switching frequency adjustment resistor (RT)

Figure 1 Boost switching frequency vs. RT

SYNCHRONIZATION

The MAP3201 can not only operate constant frequency internally, but also control switching frequency externally by using external master clock signal through SYNC Pin. The clock signal of SYNC Pin needs to be faster than internal Oscillator clock to ensure normal switching operation.

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When synchronizing multiple MAP3201 on single board, all SYNC Pin ICs of each device should be short to make all devices in sync on the Oscillator clock of the fastest device.
In this case, the number of synchronized devices differs depending on the operation frequency of Oscillator.

If this function of peer to peer synchronization is not used, the SYNC pin may be required to be open or short to GND. It is recommended to connect SYNV Pin to GND because this solution provides better immunity against parasitic noise from layout.
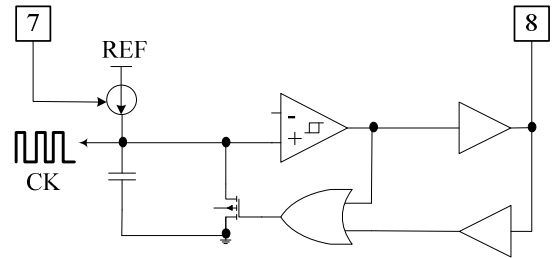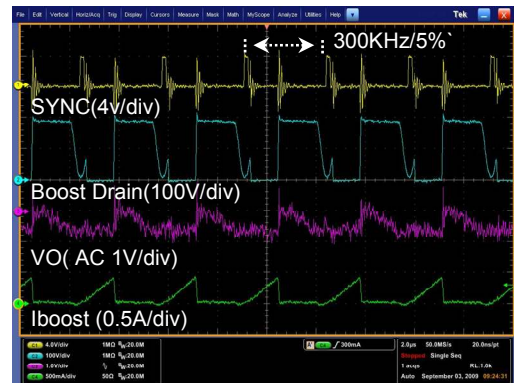

Figure 2 Internal OSC & SYNC circuit

Figure 3 Synchronization by external clock
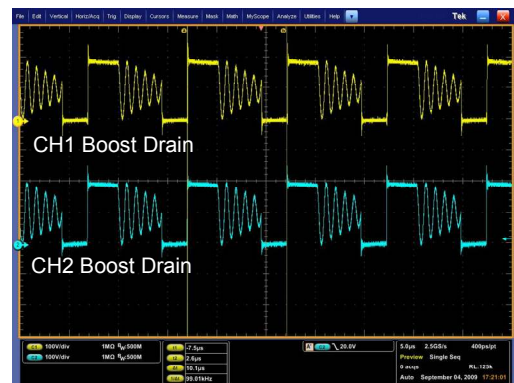(Fixed 100 KHz → 300 KHz)

Figure 4 Peer –to -peer synchronization
(Fixed 100 KHz)

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PROTECTION

The MAP3201 offers the features such as UVLO, Boost current limit, Over Voltage Protection and Short Circuit Protection of LED (SCP). OVP and SCP are operated in auto restart protection mode.

1. Under-Voltage Lock-Out (UVLO)

When VCC voltage reaches over 8V, UVLO starts operating which enables Internal 5V Regulator, making all internal control circuits including oscillator, gate driver and protection circuit ready for operation and output pin of GATE, PWMO and COMP starts operating depending on the input status of PWMI.

If VCC voltage drops below 7V during normal operation, UVLO starts operating, shutting down Internal Control Circuit and stopping operation of GATE, PWMO and COMP. It is followed by disabling of internal 5V regulator, and shut off of all IC operation.

2. Pulse by Pulse Current Limit

It will operate Pulse by Pulse current limit as voltage ratio between COMP Pin Voltage which is controlled by Gm Amp of Boost converter and CS Pin voltage which will be caused by external Boost FET.

3. Maximum Current Limit

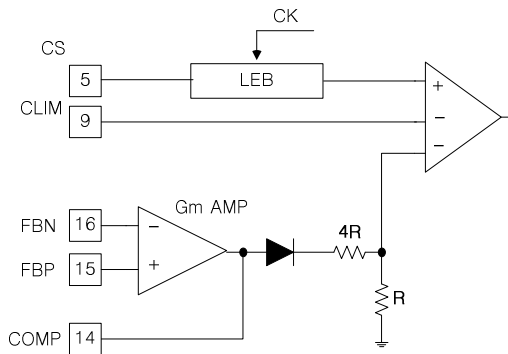Maximum current that is driven into Boost FET through CLIM Pin voltage can be set up as in Figure 5

Figure 5 Current Sense and Maximum current limit

VC, MAX: Maximum output voltage of Gm Amp
VOFF: Offset voltage of PWM comparator

$$V_{CS} = \frac{V_{C,MAX} - 0.6V}{5} - V_{OFF}$$

$$V_{CS} = V_{CLIM}$$

The equation above can be used to set up Maximum boost current when VCLIM is VCS.

4. Over Voltage Protection (OVP)

The MAP3201 offers over voltage protection in order to protect MOSFET of boost converter and external component connected to Output pin when output voltage is in abnormal condition.

OVP Circuit monitors whether output voltage is stable level or not If OVP Pin voltage reaches threshold condition (typical 3V), it can shut off the switching of GATE and PWMO and then output voltage is falling as much as the leakage current time. If the voltage of OVP Pin reaches OVP falling threshold (typical 2.7V), IC releases protection mode. In this time, protection releasing can be decided as value of capacitor with the longer discharge between auto restart time and the time of leakage current connected to output.

The over voltage protection can be decided in the following equation.

- Protection voltage:

$$V_O = 3.0 * \frac{R_{O2}}{R_{O1} + R_{O2}}$$

- Protection release voltage:
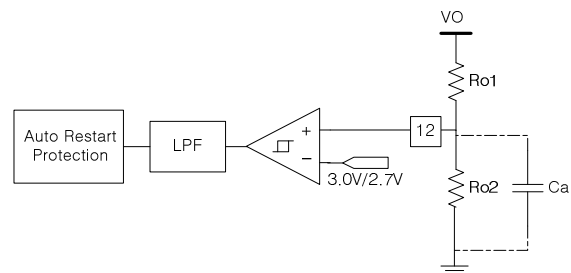
$$V_O = 2.7 * \frac{R_{O2}}{R_{O1} + R_{O2}}$$

Figure 6   Over voltage protection circuit

The MAP3201 included LPF(low pass filter) of typical 200nS in OVP circuit for better noise immunity, It may need a high noise margin when Ro1 and Ro2 use high resistance value in order to minimize Power loss.
In this case, it is recommended to add Capacitor.

5. Programmable Short Current Protection of LED (SCP)

The MAP3201 offers protection circuit to prevent short current when LED string is shorted

In Figure 7 when LED string is shorted, the voltage of FBN Pin can be calculated in the following equation

$$V_{FBN} = I_{LED} * R_{LED}$$

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The programmable SCP voltage can be set up in reference to 5V VREF in the equation below.

$$V_{ISET} = \frac{5 * R2}{R1 + R2}$$

Therefore, the SCP level can be decided by selecting the resistor value of RLED, R1 and R2.
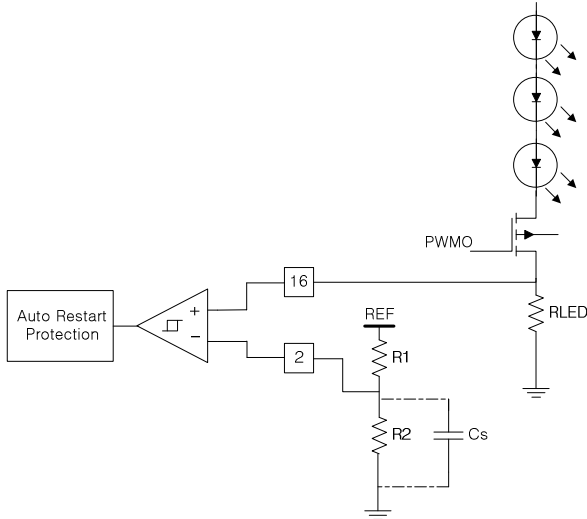

Figure 7 Programmable short current protections

SCP Circuit uses very fast comparator in order to turn off MOSFET when the abnormal condition of SCP Level is detected. Because high current can be driven into channel of MOSFET when LED string is shorted.
It is recommended to use additional ISET Cs capacitor in order to prevent abnormal SCP which is caused by noise

6. Auto-Restart Protection
The MAP3201 offers Auto Restart protection function which is recovered into normal operation mode when protection condition is cleared
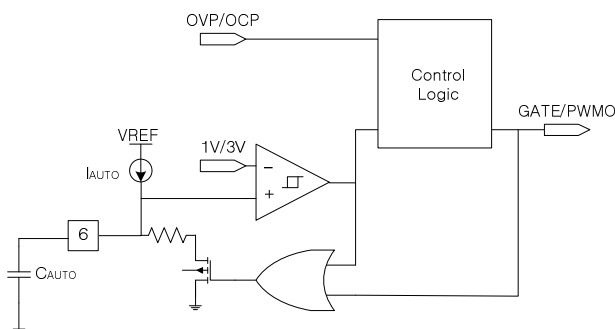

Figure 8 Auto Restart Protection circuit

Figure 8 shows auto restart protection circuit that shuts off the output of GATE switching and PWMO if protection signal is assigned to control logic circuit under OVP or SCP condition.

The timer circuit operates as the configuration of both comparator of 1V/3V Input, I$_{AUTO}$=5uA (typical) and external capacitor C$_{AUTO}$ and the restart time can be calculated in the following equation.

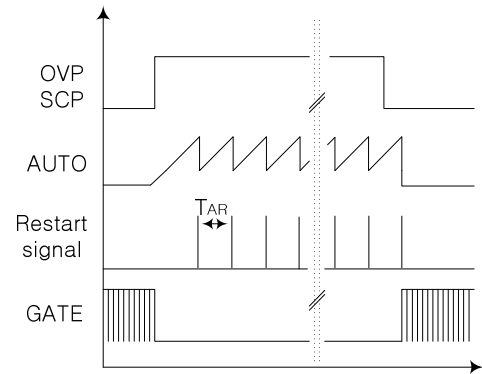$$T_{AR} = \frac{2 * C_{AUTO}}{I_{AUTO}} = 4e + 5 * C_{AUTO}$$

Figure 9 Auto Restart Protection timing diagram

On Auto-Restart Protection status, it makes restart signal of internal single pulse when the voltage of AUTO Pin is high threshold. In this case, it is recovered to normal operating mode if SCP or OVP condition is cleared. While charging AUTO pin, it recover protection when next restart signal occurs even though protection condition is cleared.

Dimming Control

1. LED Current
The MAP3201 decides LED Current setting by the value of RLED resistance which has been sensing the voltage of positive input FBP Pin of gm Amp. and LED current (V$_{FBP}$)
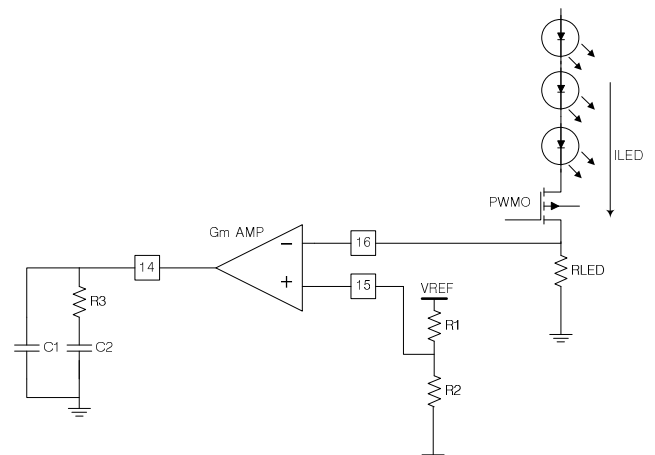

Figure 10 LED Current Setting

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In figure 10

$$V_{FBP} = \frac{V_{REF} * R2}{R1 + R2}$$

$$V_{FBN} = I_{LED} * R_{LED}$$

$$\therefore I_{LED} = \frac{5 * R2}{(R1 + R2) * R_{LED}}$$

2. PWM Dimming

The MAP3201 makes same phase PWMO output from logic PWM signal of PWMI using intenral Level shift. PWMO of operating voltage level is between GND and VCC.

Inductor Selection

Inductor value should be decided before system design.
Because the selection of the inductor affects the operating mode of CCM (Continuous current mode) or DCM (Discontinuous current mode).
In CCM operation, indutor size should be bigger, even though the ripple current and peak current of inductor can be small.
In DCM operation, even ripple current and peak current of inductor should be large while the inductor size can be smaller so that it is more effective in BLU of TV and Notebook application.

The MAP3201 was designed for DCM operation.
In CCM operation, sub-harmonic oscillation may occur if duty cycle exceeds over 50%. Because there is no slope compensation functions.

The following is the equation to calculate Max.Value of Inductor in DCM operation.

$$L_{(max)} = \frac{[(1-D)^2 * D * R_{O(max)} * T_{s(min)}]}{2}$$

$$* R_{O(max)} = Maximum\_Output\_\text{Im}pedance$$

$$* T_{S(min)}) = Minimum\_Switching\_period$$

Closed Loop Network Selection

The MAP3201 controls in peak current mode. Current mode easily achieves compensation by consisting simple single Pole from Double Pole that LC filer makes at Voltage mode
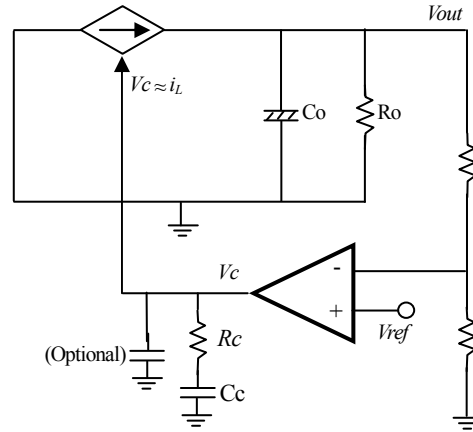

Figure 11 Current mode Loop Compensation

1. Select fc (Crossover frequency)

In general, crossover frequency is selected from 1/3 ~ 1/6 range of the switching frequency. If fc is large, there is possibility of oscillation to occur, although time response gets better.
On the other hand, if fc is small, time response will be bad, while it has improved stability, which may cause over shoot or under shoot in abnormal condition.
It should be noted that fc should be set at smaller location than RHP Zero.

$$f_{RHP} = \frac{Ro * (1-D)^2}{2\pi * L} \quad \text{(Boost)}$$

2. Select fPO

$$f_{PO} = f_C * G_O$$

$$(G_O = DC \text{ Gain of plant} = \frac{A}{B})$$

$$A = \frac{1}{\frac{2}{R} + \frac{(m-0.5)*(1-D)^3}{L*F}}$$

Selecting approximately m = 1.4

$$B = R_S * (1-D)$$

$$R_S = \text{Sensing Resistor}$$

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3. Select Pole and Zero

$$f_{PO} = \frac{1}{2\pi * \dfrac{C_C}{Y * G_{EA}}}$$

$G_{EA} =$ Gm-Amp Transconductance

$$Y = Attenuation - Ratio = \frac{V_{FPN}}{V_O}$$

$$f_{Z1} = \frac{1}{2\pi * R_C * C_C}$$

Zero is set at the same location of output pole. In system design, if ESR of output capacitor is large, Pole should be set at same frequency in order to compensate The Zero of ESR.

$$f_{P1(OP)} = \frac{1}{2\pi * R_C * C_{OP}}$$

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