M74HCT651

OCTAL BUS TRANSCEIVER/REGISTER WITH 3 STATE OUTPUTS (INVERTING)

- HIGH SPEED:
  f_{MAX} = 55 MHz (TYP.) at V_{CC} = 4.5V
- LOW POWER DISSIPATION:
  I_{CC} = 4µA(MAX.) at T_A=25°C
- COMPATIBLE WITH TTL OUTPUTS :
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 6mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 651

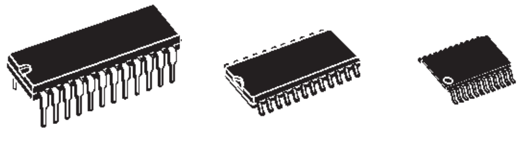
DESCRIPTION

The 74HCT651 is an advanced high-speed CMOS OCTAL BUS TRANSCEIVER AND REGISTER (3-STATE) fabricated with silicon gate C^2MOS technology.

This device consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. Enable GAB and $\overline{GBA}$ are provided to control the transceiver functions. Select AB(SAB) and select BA(SBA) control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transition at the appropriate clock pins (CLOCK AB or CLOCK BA) regardless of the select or enable control pins. When select AB and select BA are in the real time transfer mode, it is also possible to store data without using the internal D type flip-flops by simultaneously enabling GAB and GBA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

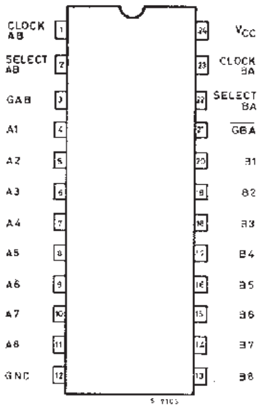
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

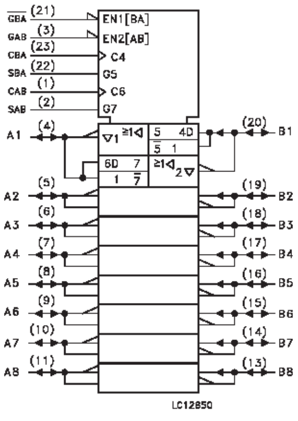


ORDER CODES

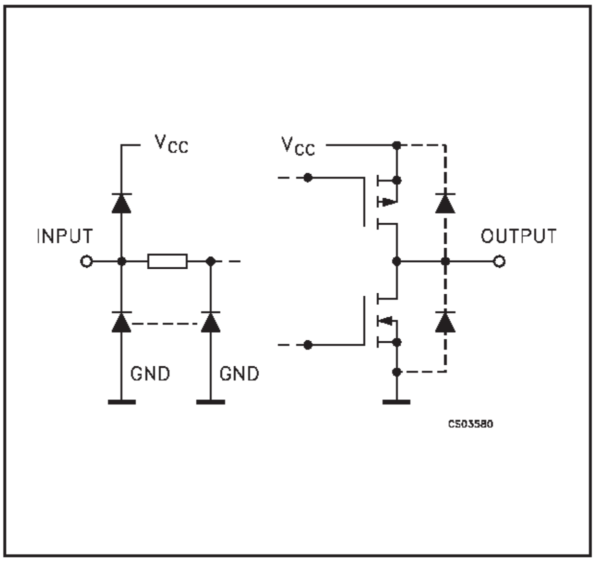
PACKAGE	TUBE	T & R
DIP	M74HCT651B1R	
SOP	M74HCT651M1R	M74HCT651RM13TR
TSSOP		M74HCT651TTR

PIN CONNECTION AND IEC LOGIC SYMBOLS





INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	CAB	A to B Clock Input (LOW to HIGH, Edge-Triggered)
2	SAB	Select A to B Source Input
3	GAB	Direction Control Input
4, 5, 6, 7, 8, 9, 10, 11	A1 to A8	A Data Inputs/Outputs
20, 19, 18, 17, 16, 15, 14, 13	B1 to B8	B Data Inputs/Outputs
21	$\overline{GBA}$	Output Enable Input (Active LOW)
22	SBA	Select B to A Source Input
23	CBA	B to A Clock Input (LOW to HIGH, Edge Triggered)
12	GND	Ground (0V)
24	V_{CC}	Positive Supply Voltage

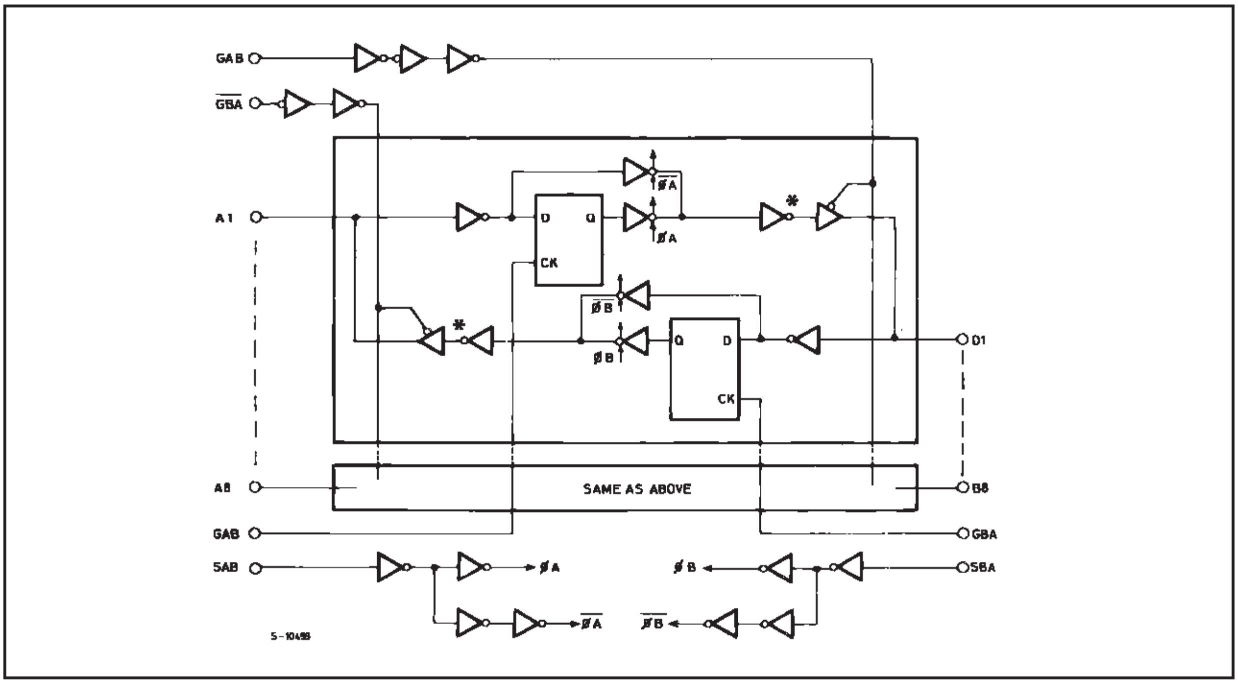
TRUTH TABLE

GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A	B	FUNCTION
L	H					INPUTS	INPUTS	Both the A bus and the B bus are inputs
		X	X	X	X	Z	Z	The Output functions of the A and B bus are disabled
		↑	↑	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs.
L	L					OUTPUTS	INPUTS	The A bus are outputs and the B bus are inputs
		X*	X	X	L	L	H	The data at the B bus are displayed at the A bus
						H	L	
		X*	↑	X	L	L	H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to internal flip-flop on low to high transition of the clock pulse
						H	L	
		X*	X	X	H	Qn	X	The data stored to the internal flip-flop are displayed at the A bus.
		X*	↑	X	H	L	H	The data at the B bus are stored to the internal flip-flop on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.
						H	L	
H	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L	H	The data at the A bus are displayed at the B bus
						H	L	
		↑	X*	L	X	L	H	The data at the A bus are displayed at the B bus. The data of the A bus are stored to the internal flip-flop on low to high transition of the clock pulse.
						H	L	
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus
		↑	X*	H	X	L	H	The data at the A bus are stored to the internal flip-flop on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus.
			X*	H	X	H	L	

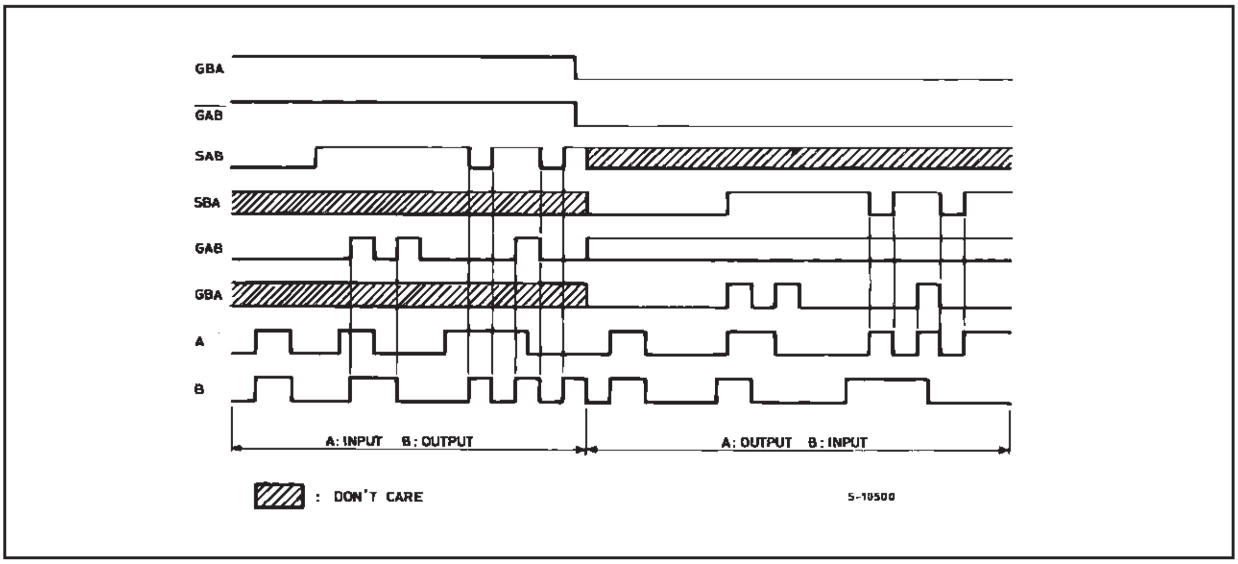
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A	B	FUNCTION
H	L					OUTPUTS	OUTPUTS	
		X	X	H	H	Qn	Qn	The data stored to the internal flip-flops are displayed at the A and B bus respectively.
		↑	↑	H	H	Qn	Qn	The output at the A bus are displayed at the B bus, the output at the B bus are displayed at the A bus respectively

X : Don't Care
Z : High Impedance
Qn : The data stored to the internal flip-flops by most recent low to high transition of the clock inputs
* : The data at the A and B bus will be stored to the internal flip-flops on every low to high transition of the clock inputs.

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5		2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		V
			I_O=-6.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	I_O=20 µA		0.0	0.1		0.1		0.1	V
			I_O=6.0 mA		0.17	0.26		0.33		0.40	
I_I	Input Leakage Current	5.5	$V_I = V_{CC}$ or GND			± 0.1		± 1		± 1	µA
I_{OZ}	High Impedance Output Leakage Current	5.5	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND			± 0.5		± 5		± 10	µA
I_{CC}	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND			4		40		80	µA
ΔI_{CC}	Additional Worst Case Supply Current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O = 0			2.0		2.9		3.0	mA

(*) Applicable Only to GAB, $\overline{GBA}$, CAB, CBA, SAB, SBA Input

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6ns)

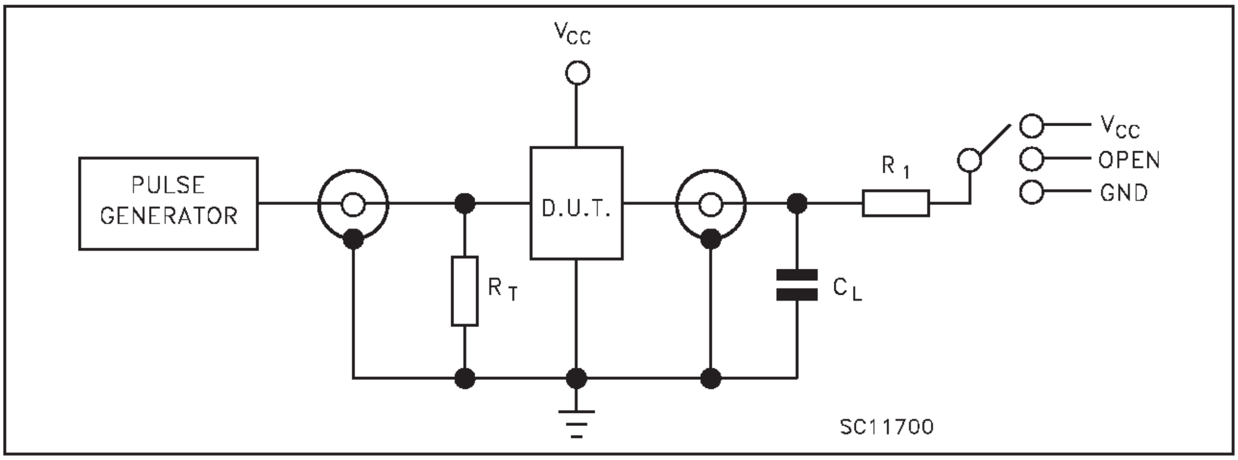
Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5	50			7	12		15			ns
t_{PLH} t_{PHL}	Propagation Delay Time (BUS - BUS)	4.5	50			20	30		38			ns
		4.5	150			25	38		48			
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - BUS)	4.5	50			29	44		55			ns
		4.5	150			34	52		65			
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT - BUS)	4.5	50			24	34		43			ns
		4.5	150			29	42		53			
t_{PZL} t_{PZH}	High Impedance Output Enable Time	4.5	50	R_L = 1 KΩ		22	33		41			ns
		4.5	150	R_L = 1 KΩ		27	41		51			
t_{PLZ} t_{PHZ}	High Impedance Output Disable Time	4.5	50	R_L = 1 KΩ		24	35		44			ns
f_{MAX}	Maximum Clock Frequency	4.5	50		31	55		25				MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width	4.5	50			8	15		19			ns
t_s	Minimum Set-Up Time	4.5	50			3	10		13			ns
t_h	Minimum Hold Time	4.5	50				5		5			ns

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance				5	10		10		10	pF
$C_{I/O}$	Bus Terminal Capacitance				13						pF
C_{PD}	Power Dissipation Capacitance (note 1)				38						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per channel)

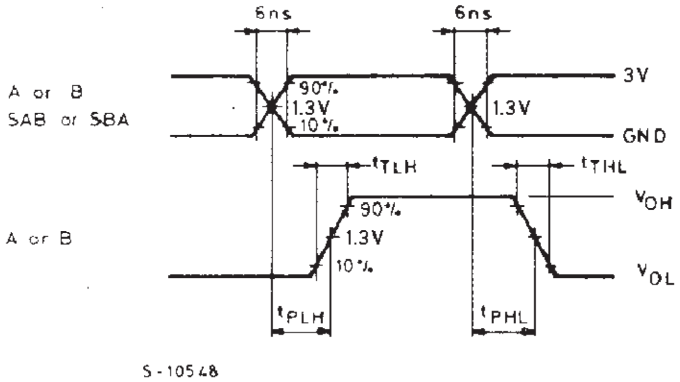
TEST CIRCUIT



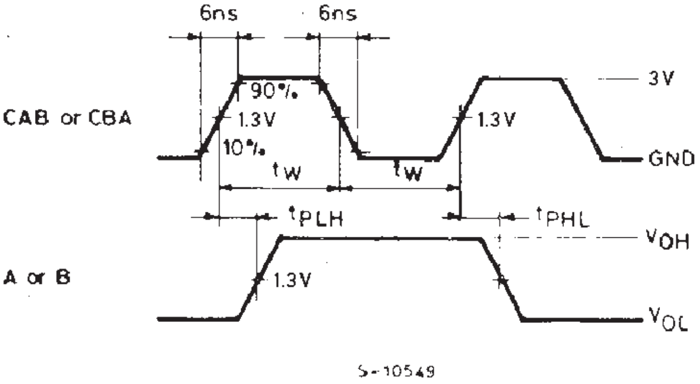
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC}
t_{PZH}, t_{PHZ}	GND

C_L = 50pF/150pF or equivalent (includes jig and probe capacitance)
R_1 = 1KΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

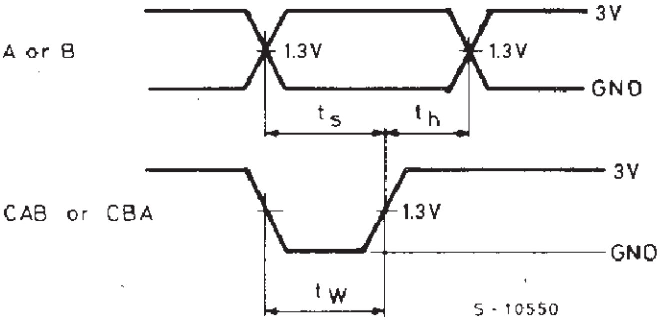
WAVEFORM 1 : PROPAGATION DELAY TIME(f=1MHz; 50% duty cycle)



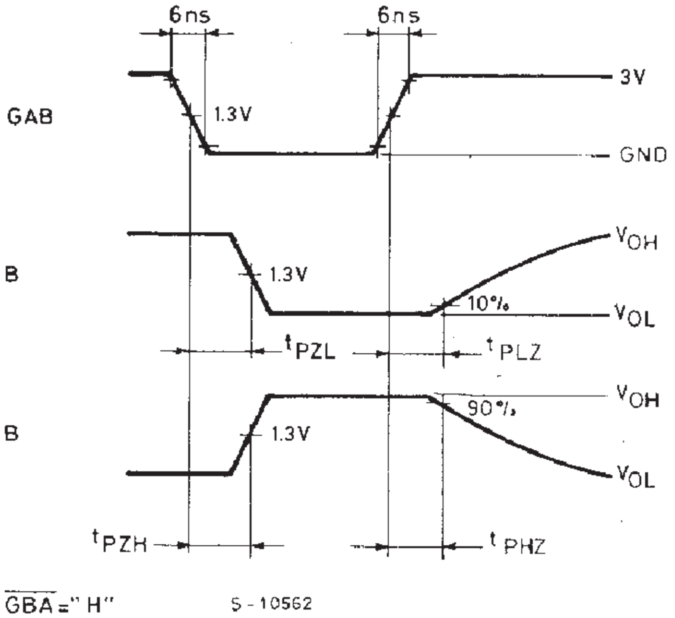
WAVEFORM 2 : MINIMUM PULSE WIDTH, PROPAGATION DELAY (f=1MHz; 50% duty cycle)



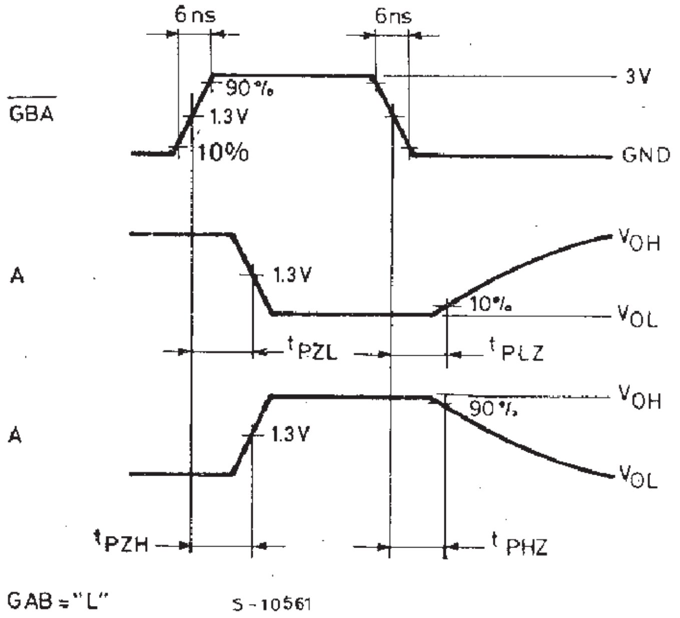
WAVEFORM 3 : MINIMUM SETUP AND HOLD TIME ((f=1MHz; 50% duty cycle)



WAVEFORM 4 : OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)

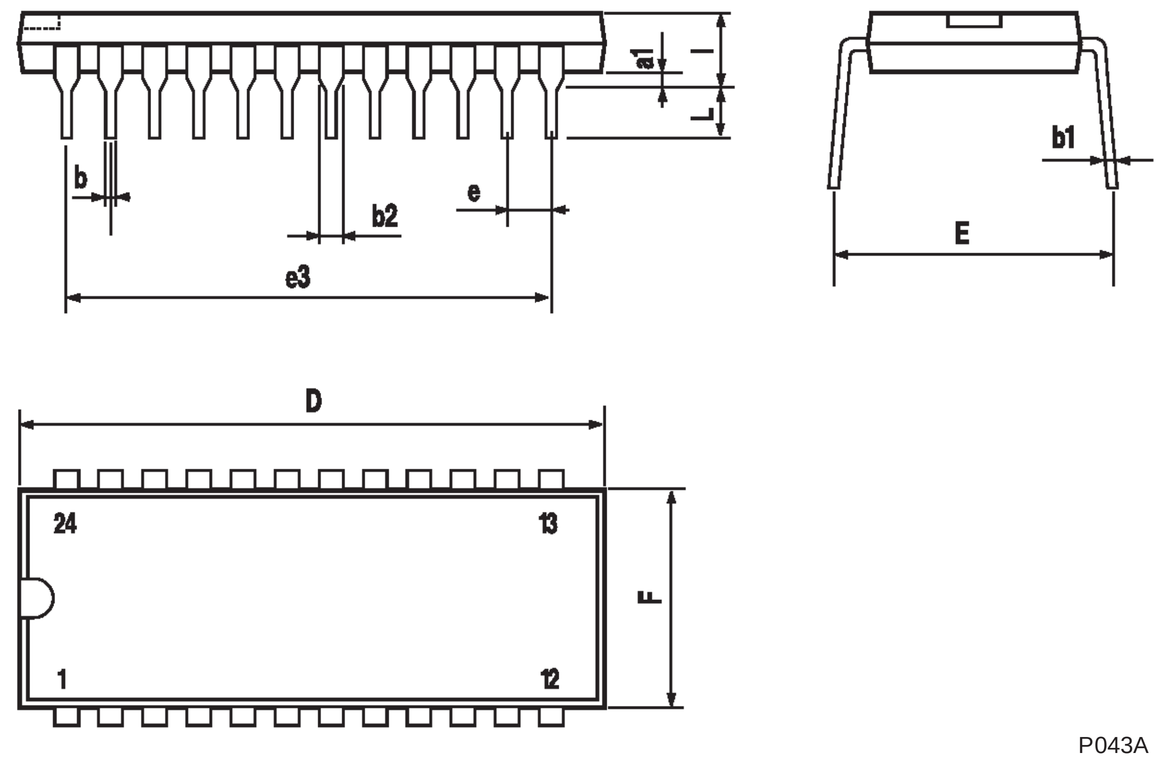


WAVEFORM 5 : OUTPUT ENABLE AND DISABLE TIME(f=1MHz; 50% duty cycle)



Plastic DIP-24 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.500	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	



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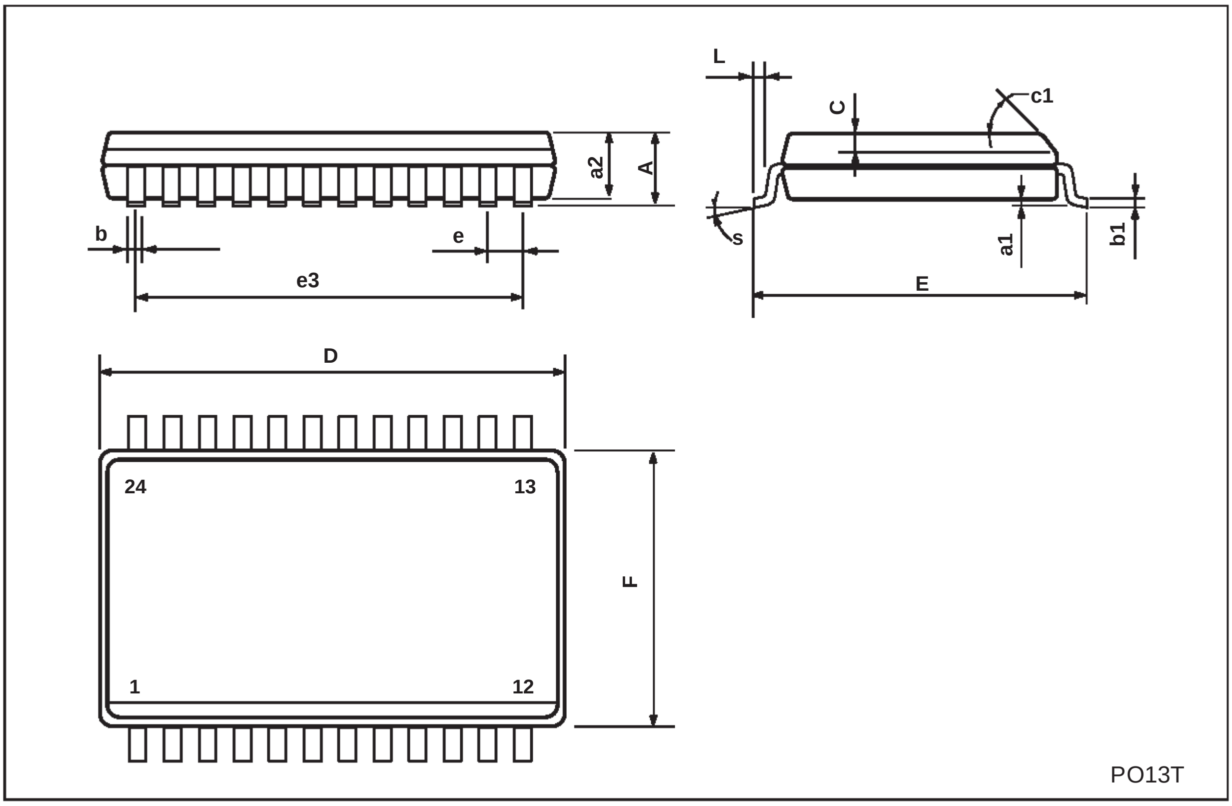
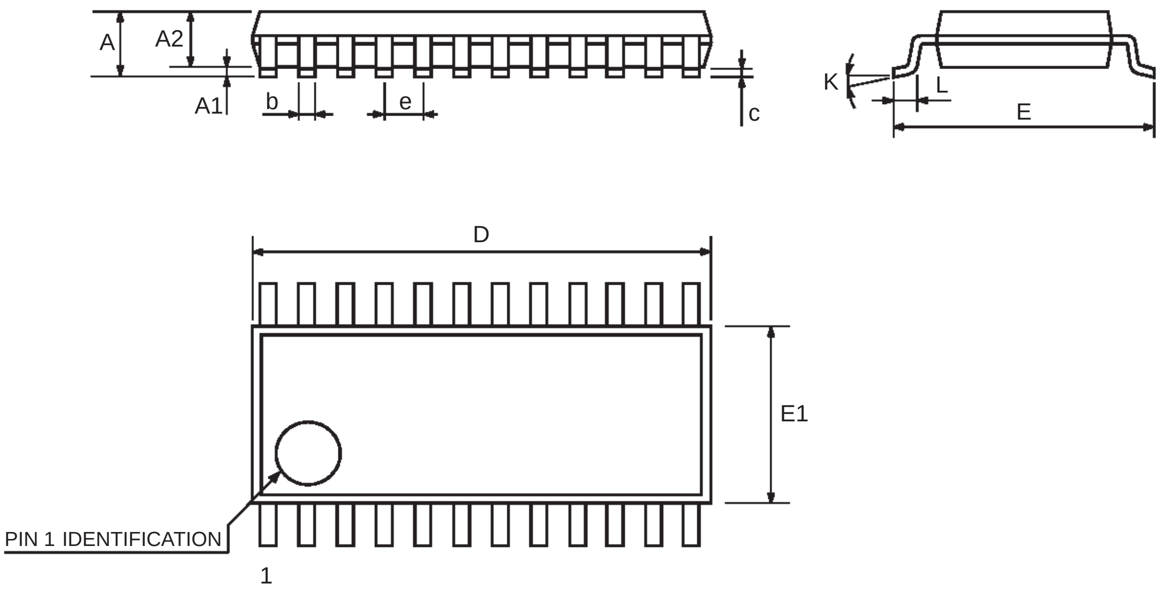
SO-24 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	8° (max.)					



TSSOP24 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	7.7		7.9	0.303		0.311
E	6.25		6.5	0.246		0.256
E1	4.3		4.5	0.169		0.177
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.50		0.70	0.020		0.028



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