LSI COMPUTER SYSTEMS INC.
Manufacturers of Custom and Standard LSI Circuits.
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LS7228/LS7229 | ADDRESS DECODER/TWO PUSHBUTTON DIGITAL LOCK

REVISED NOVEMBER 1985

FEATURES:
- Stand alone lock logic
- 9 bit code determined by 9 parallel inputs
- Two options of code input available:
  LS7228 – Dual train pulsed input
  LS7229 – Two momentary switches
- Out of sequence disabling circuit
- Current source lock control output
- External controlled delay to set maximum interpulse time.
- Single power supply operation (2.5V to 15.0V)
- Low standby current (15uA maximum)
- 16 pin dual-in-line plastic package
- Cascadable

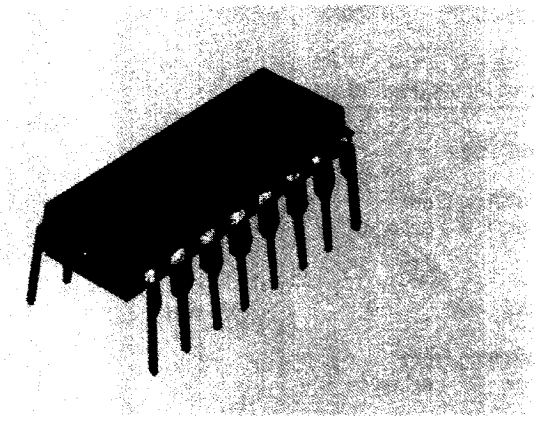
DESCRIPTION:
LS7228/LS7229 are monolithic ion implanted MOS encoder circuits. Each circuit includes logic for interpretation of correct sequential key closure or pulse input and a momentary lock control output. An out of sequence detection will disable any further insertions, and a new sequence may be reapplied after a delay time, determined by an external R/C time constant.

The LS7228 utilizes a dual train input format where the input "one's" data is applied to pin 13 and the input "zero's" is applied to pin 14. The common input (pin 15) is not used. (See figure 4). The LS7229 utilizes two momentary switches and pins 13, 14 and 15 in a manual operating mode.

PROGRAMMING 9 BIT CODE:
Pin 1 (leading bit) and through Pin 9 (end bit) with 512 (leading bit) different combinations. To program a Logic 1 the pin is left floating. To program a Logic 0 the pin is tied to VDD (GND).

LOCK CONTROL OUTPUT:
Code entry is made at the one's port or the zero's port with logical one levels (+ volts) and returned to the logical zero level (GND) in sequential order. The lock control output will change to a logical one after the last correct bit entry returns to logical zero and will remain at a logical one for the period of the external R/C delay. If it is desired to maintain a constant logical one output, a tenth entry either at the one or zero port must be held at a logical one level.

STANDBY AND OPERATING CURRENT:
1. Upon application of supply voltage, the standby section is activated, leaving the remaining portion of the circuit unenergized.



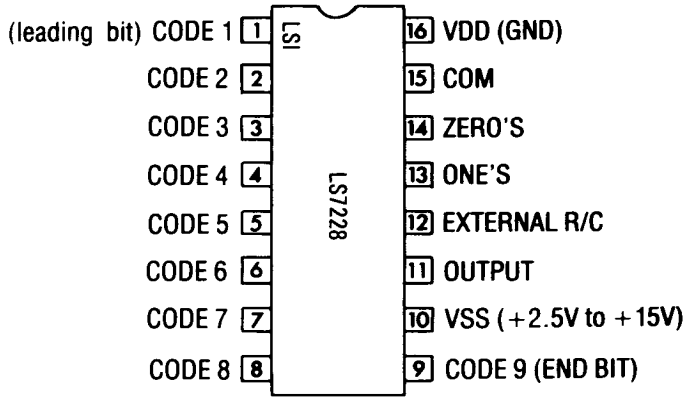


Figure 1
TOP VIEW
Standard 16 pin DIP

STANDBY AND OPERATING CURRENT (cont'd.)
(Standby current is 15 μA max.)
2. The entire circuit is energized by entering the first bit in the code pattern and will be energized only during the selected external R/C delay time, every bit entry will refresh the external delay time. (Operating current is 5mA max.)

CASCADING:
See Figure 4.

DESCRIPTION OF INTERNAL OPERATION: (See fig. 3)
When entering code to either the one's port or the zero's port, an

external capacitor is charged and an internal inhibit is removed to allow further code insertion, providing that the previous insertion was the correct code. In effect, a one is transmitted through the nine BIT shift register if the input sequence agrees with the program applied to pins one through nine.

If an incorrect insertion occurs, the one is prevented from advancing even though further code insertions occur, keeping the external capacitor fully charged. Only the removal of code entrys will allow the external capacitor to discharge and reset the error logic, thereby permitting a new attempt at entering the correct code.

MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_a	−25 to +70	°C
Voltage (any pin to V_{SS})	V_{max}	−30 to +0.5	VOLTS

DC ELECTRICAL CHARACTERISTICS

INPUT SPECIFICATIONS

INPUT VOLTAGE

Program Inputs (Pins 1 through 9)

	MIN.	MAX.	UNITS
Logical "1"	V_{SS}-0.5	V_{SS}	VOLTS
Logical "0"	0	V_{SS}−2.5	VOLTS

Serial Inputs (Pins 13, 14, 15)

	SYMBOL	V_{SS} (VDC)	MIN	TYP.	MAX.	UNITS
Input Logic	V_{IL}	2.5	1.9	1.65	2.5	VDC
"1"		5.0	4.3	4.0	5.0	VDC
Switching From		9.0	8.0	7.6	9.0	VDC
Logic ("0") to Logic ("1")		12.0	11.0	10.6	12.0	VDC
		15.0	14.0	13.6	15.0	VDC
Input Logic	V_{IH}	2.5	0	.7	.3	VDC
"0"		5.0	0	1.5	.5	VDC
Switching From		9.0	0	2.0	1.0	VDC
Logic ("1") to Logic ("0")		12.0	0	4.0	1.5	VDC
		15.0	0	4.5	2.0	VDC

External R Applied To Pin 12

	SYMBOL	V_{SS}	MIN	TYP.	MAX.	UNITS
	R	2.5	33	—	3300	K Ω
		5.0	27	—		K Ω
		9.0	22	—		K Ω
		12.0	15	—		K Ω
		15.0	10	—	3300	K Ω

External R/C Input (Pin 12)

	SYMBOL	V_{SS} (VDC)	TYP.	UNITS
Input Logic		2.5	1.6	VDC
"1"		5.0	3.8	VDC
Switching From		9.0	7.5	VDC
Logic ("0") to Logic ("1")		12.0	10.4	VDC
		15.0	13.4	VDC

	SYMBOL	V_{SS}	TYP.	UNITS
Input Logic		2.5	.6	VDC
"0"		5.0	1.2	VDC
Switching From		9.0	2.2	VDC
Logic ("1") to Logic ("0")		12.0	4.5	VDC
		15.0	6.0	VDC

Input Current To V_{SS} ($V_{IN} = V_{DD}$)

	TYPICAL	MAX.	UNITS
Program Inputs	Standby 1	—	nA
(Pins 1 through 9)	Operating 2	−5	uA

Input Current To V_{DD} (V_{IN} to V_{SS})

Serial Input			
(Pins 13 and 14)	3	5	uA
(Pin 15)	1.5	3	uA

MAX FREQUENCY - vs - OPERATING VOLTAGE FOR DUAL TRAIN OPERATION is Linear with respect to capacitor size applied to pin 12. See Dynamic Electrical Characteristics (See below)

OUTPUT SPECIFICATIONS

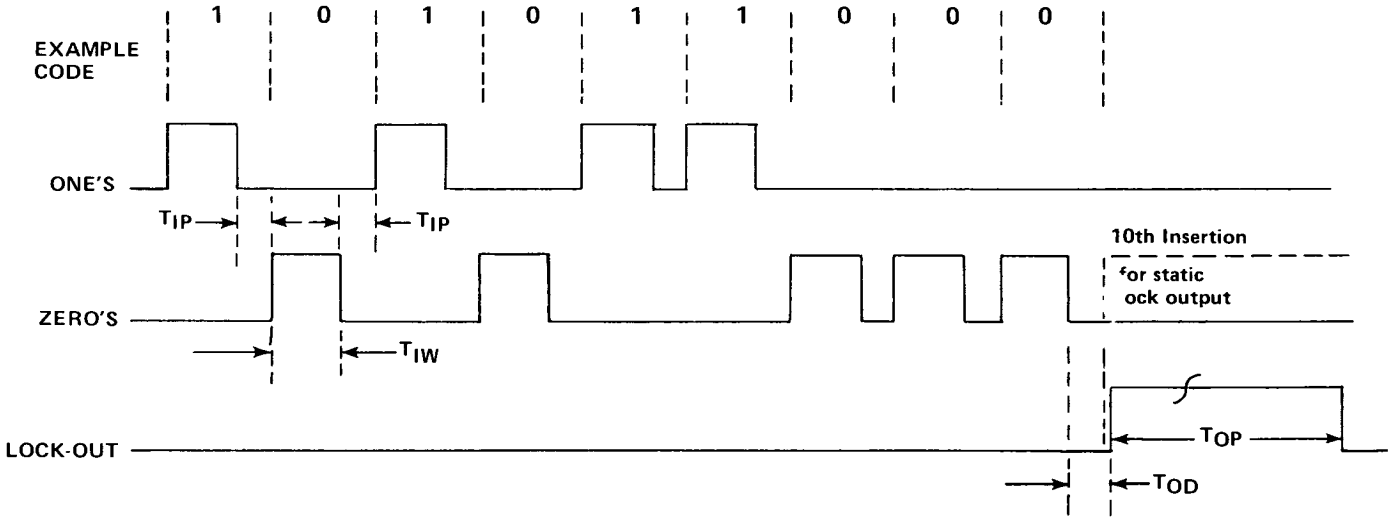
LOCK CONTROL OUTPUT PIN 11

SOURCE CURRENT	V_{SS}	MIN.	TYP.	MAX.	UNITS
$V_{OUT} = V_{SS}$ - .5 VDC	2.5VDC	1.4	2.5	3.5	mA
	5.0VDC	3.0	5.6	8.0	mA
	9.0VDC	5.0	9.0	13.0	mA
	12.0VDC	6.0	11.0	16.0	mA
	15.0VDC	7.0	13.0	18.0	mA
$V_{OUT} = V_{SS}$ - 1.0 VDC	2.5VDC	2.2	4.0	5.6	mA
	5.0VDC	6.0	11.0	16.0	mA
	9.0VDC	10.0	18.0	25.0	mA
	12.0VDC	12.0	22.0	31.0	mA
	15.0VDC	14.0	26.0	36.0	mA
$V_{OUT} = V_{SS}$ - 1.5 VDC	2.5VDC	2.7	5.0	7.0	mA
	5.0VDC	8.0	14.0	20.0	mA
	9.0VDC	14.0	26.0	36.0	mA
	12.0VDC	18.0	33.0	46.0	mA
	15.0VDC	20.0	38.0	53.0	mA

NOTE: Pin 11 (Lock Control Output) is only a current source. Use a resistor to ground (V_{DD}) if driving capacitor load.

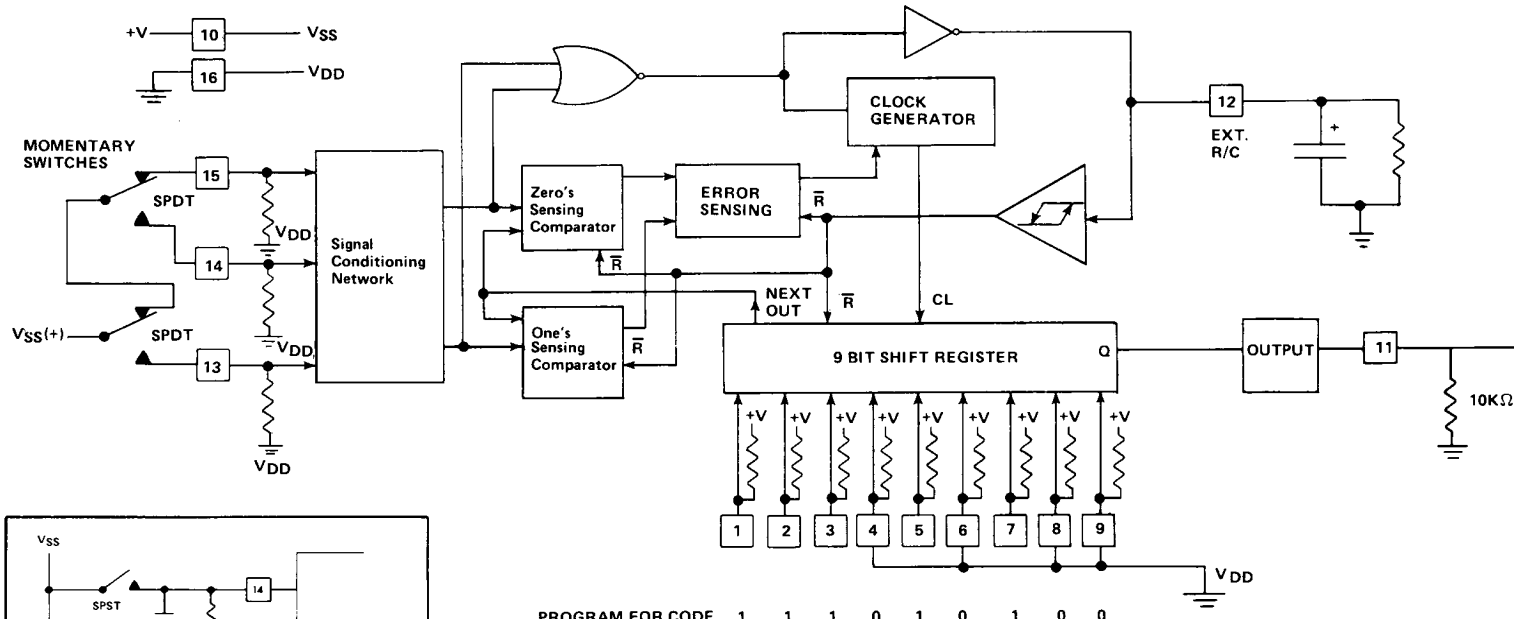
DYNAMIC ELECTRICAL CHARACTERISTICS (See Fig. 2)

PARAMETER	SYMBOL	V_{SS}	MIN.	TYP.	MAX.	UNITS
Input Pulse Width (with C on Pin 12 ≤.01 uf)	T_{IW}	2.5	50	—	—	usec
		5.0	80	—	—	usec
		9.0	120	—	—	usec
		12.0	160	—	—	usec
		15.0	200	—	—	usec
Output Delay	T_{OD}	—	20	40	70	usec
Output Pulse Width T_{OP} typically 1.25 time constants of external RC network applied to Pin 12						
Input Interpulse time	T_{IP}		30	—	T_{OP}	usec

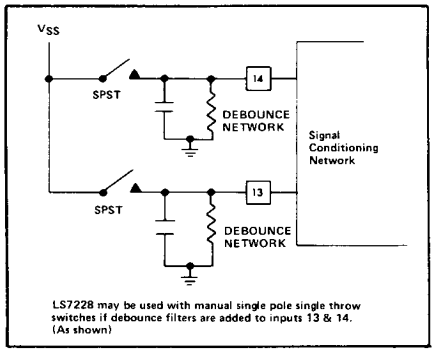


TIMING DIAGRAM

Figure 2



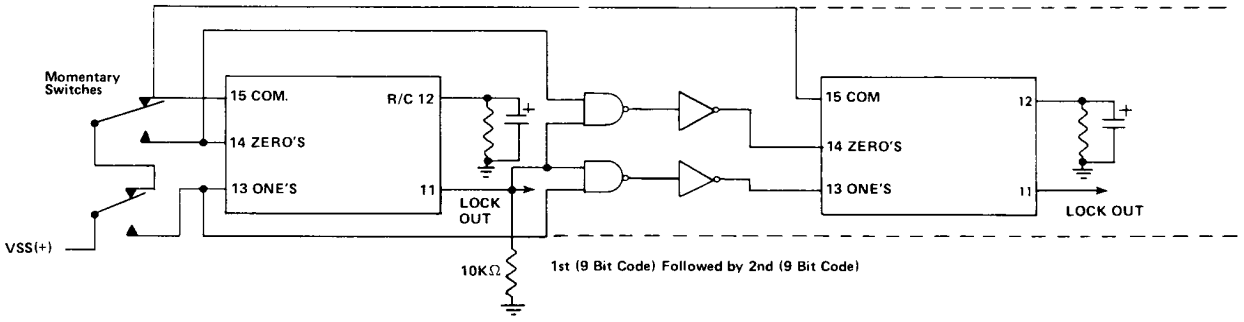
LS7229 BLOCK DIAGRAM



LS7228 may be used with manual single pole single throw switches if debounce filters are added to inputs 13 & 14. (As shown)

Figure 3

DUAL SWITCH CASCADING SERIES (LS7229)



DUAL TRAIN CASCADING SERIES PARALLEL (LS7228)

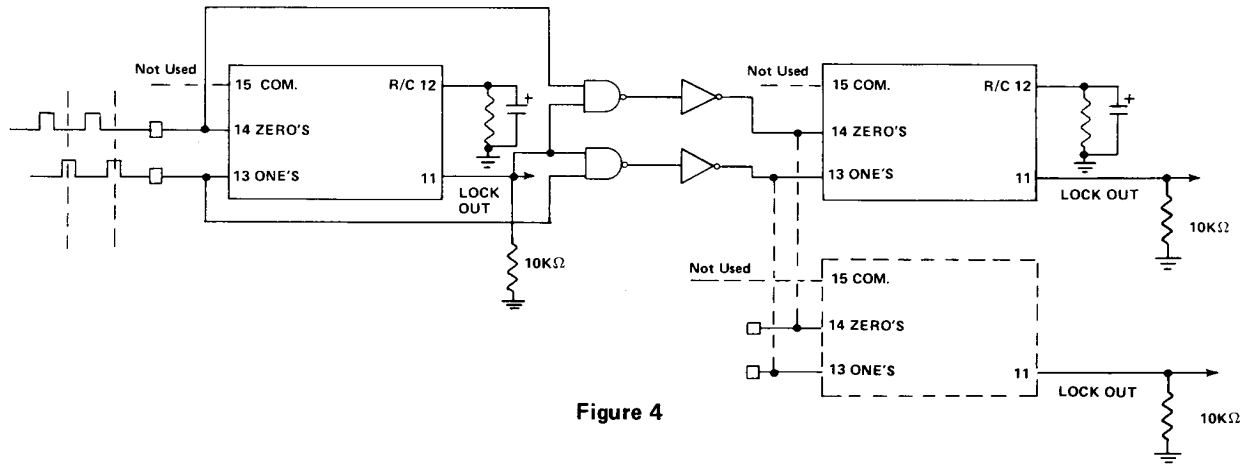


Figure 4