LPC-P2106 PROTOTYPE BOARD FOR
LPC2106 ARM7TDMI-S MICROCONTROLLER

Features:
- MCU: 16/32 bit LPC2106 with 128K Bytes Program Flash, 64K Bytes RAM, RTC, 2x UARTs, I2C, SPI, 2x 32bit TIMERS, 7x CCR, 6x PWM, WDT, 5V tolerant I/O, up to 60MHz operation
- standard JTAG connector with ARM 2x10 pin layout for programming/debugging with ARM-JTAG
- push BUTTON with pullup
- status LED
- two on board voltage regulators 1.8V and 3.3V with up to 800mA current
- Power plug-in jack
- single power supply: +5-9VAC/DC required
- power supply filtering capacitor
- RS232 interface circuit
- RESET circuit
- RESET button
- DEBUG jumper for JTAG enable
- BSL jumper for Bootloader enable
- RTCK pullup resistor
- 14.7456 Mhz crystal allow easy communication setup (4x PLL = 58,9824 Mhz CPU clock)
- extension headers for all uC ports
- PCB: FR-4, 1.5 mm (0,062"), green soldermask, white silkscreen component print
- prototype PCB area with +3.3V and GND bus
- Four mounting holes
- Dimensions: 77x100 mm (3.9x3.05")

Supported devices:
Philips Semiconductors Inc. LPC2106 16/32 bit ARM7TDMI-S™

JTAG interface:
The JTAG connector is 2x10 pin with 0,1" step and ARM recommended JTAG layout. PIN.1 is marked with square pad on bottom and arrow on top.

Note: to enable JTAG interface DBG jumper should be shorted <u>at the time of POWER UP</u>.

Important: when JTAG is enabled P0.18-P1.31 ports take their JTAG alternative function no matter of PINSEL register value, so during debugging with JTAG these ports are not available for the user program.

JTAG signals description:
PIN.1 (VTREF) Target voltage sense. Used to indicate the target's operating voltage to the debug tool.

PIN.2 (VTARGET) Target voltage. May be used to supply power to the debug tool.

PIN.3 (nTRST) JTAG TAP reset, this signal should be pulled up to Vcc in target board.

PIN4,6, 8, 10,12,14,16,18,20 Ground. The Gnd-Signal-Gnd-Signal strategy implemented on the 20-way connection scheme improves noise immunity on the target connect cable.

PIN.5 (TDI) JTAG serial data in, should be pulled up to Vcc on target board.

PIN.7 (TMS) JTAG TAP Mode Select, should be pulled up to Vcc on target board.

PIN.9 (TCK) JTAG clock.

PIN.11 (RTCK) JTAG re-timed clock. Implemented on certain ASIC ARM implementations the host ASIC may need to synchronize external inputs (such as JTAG inputs) with its own internal clock.

PIN.13 (TDO) JTAG serial data out.

PIN.15 (nSRST) Target system reset.

PIN.17 (DBGRQ) Asynchronous debug request. DBGRQ allows an external signal to force the ARM core into debug mode, should be pull down to GND.

PIN.19 (DBGACK) Debug acknowledge signal. The ARM core acknowledges debug-mode in response to a DBGRQ input.

JTAG connector layout:

```
          ARM_JTAG

  VREF    1         2  VTARGET
  NTRST   3         4  GND
  TDI     5         6  GND
  TMS     7         8  GND
  TCK     9        10  GND
  RTCK   11        12  GND
  TDO    13        14  GND
  RST    15        16  GND
  DBGRQ  17        18  GND
  DBGACK 19        20  GND

        (PCB TOP VIEW)
```

Development boards for ARM, AVR, MSP430 and PIC microcontrollers **http://www.olimex.com/dev**

Power supply:

Power supply is made with two LDO adjustable voltage regulators LM1117. Input voltage should be in range 5-9VAC/DC.

RS232 interface:

LPC2106 have two RS232 channels. Only Channel 0 is via MAX3232 IC to SUB D 9 pin connector. Channel 0 with TXD0 and RXD0 is used by the Bootloader program to program LPC2106 Flash memory without external programmer. Channel 1 is general purpose RS232 channel and may be used by user program.

RESET:

Reset circuit is made by simple external RC group. There is possibility to apply RESET externally by the small RESET pushbutton on the board.

Oscillator:

14.7456 Mhz crystal is used for LPC2106 as it allows easy setup on any communication speed This makes programming with Philips ISP utility possible at any speed up to 115Kbps.

Bootloader:

The Bootloader program is enabled when BSL jumper is shorted at time of power up. In this case Bootloader takes the program control and user may download Flash memory with Philips ISP programming utility. Note that if you want to run code in Flash memory BSL jumper should be open at time of power up, otherwise Bootloader will stay in control and will not allow program in Flash to run.

Board layout:
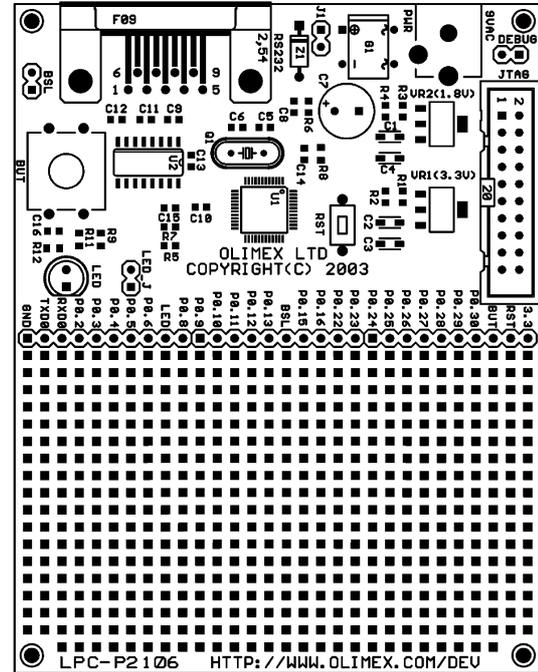
Ordering codes:

LPC-P2106   - assembled and tested with LPC2106 microcontroller

RS232

GND

C13 100n
C12 100n

U2 MAX3232
R1IN T1OUT
R2IN T2OUT
C1+
C1-
C2+
C2-
V+
V-
T1IN
T2IN
R1OUT
R2OUT

U2PWR
3.3V
C15 100n
15nd
vd16

C11 100n
C9 100n

GND
RXD0 TXD0

GND

9VAC
PWR

DB104
G1
GND

1N4733
Z1
220uF/25VDC
C7
J1
1
2
GND

C3 10uF
R2 390
VR1(3.3V) LM1117
IN OUT
ADJ/GND
R1 240
3.3V
C2 10uF
C14 100n

GND

C4 10uF
R4 100
VR2(1.8V) LM1117
IN OUT
ADJ/GND
R3 220
C1 10uF
1.8V

DEBUG
1 2

R5 22K
R7 10k
3.3V 3.3V 3.3V
R6 10k

C8 100n
RST

C5 39pF
C6 39pF
14.7456MHz
Q1
GND

C10 100n

GND

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U1
LPC2106

VSS4
VSS3
VSS2
VSS1
VDD3-2(I/O)
VDD3-1(I/O)
VDD1.8(CORE)
X2
X1
NC1
NC2
NC3
NC4
RTCK
DBGSEL
RST

P0.0/TXD0/PWM1
P0.1/RXD0/PWM3
P0.2/SCL/CAP0.0
P0.3/SDA/MAT0.0
P0.4/SCK/CAP0.1
P0.5/MISO/MAT0.1
P0.6/MOSI/CAP0.2
P0.7/SSEL/PWM2
P0.8/TXD1/PWM4
P0.9/RXD1/PWM6
P0.10/RTS1/CAP1.0
P0.11/CTS1/CAP1.1
P0.12/DSR1/MAT1.0
P0.13/DTR1/MAT1.1
P0.14/DCD1/EINT1
P0.15/RI1/EINT2
P0.16/EINT0/MAT0.2
P0.17/CAP1.2/TRST
P0.18/CAP1.3/TMS
P0.19/MAT1.2/TCK
P0.20/MAT1.3/TDI
P0.21/PWM5/TDO
P0.22/TRACECLK
P0.23/PIPESTAT0
P0.24/PIPESTAT1
P0.25/PIPESTAT2
P0.26/TRACESYNC
P0.27/TRACEPKT0/TRST
P0.28/TRACEPKT1/TMS
P0.29/TRACEPKT2/TCK
P0.30/TRACEPKT3/TDI
P0.31/EXTIN0/TDO

BUT
R11 10K
3.3V
C16 100n

R8 4.7K
3.3V
LED
R12 390
LED_J
3.3V

JTAG

BSL
R9 10K
3.3V

EXT3

EXT2

EXT1

GND