8K x 8 Bit EEPROM with Latches and Auto-Write

FEATURES

- **Simple Byte Write**
  - **Fast Byte Write Time**
  - **Single TTL Level Write Signal**
  - **Latched Address and Data**
  - **Automatic Internal Erase-before-Write**
  - **Automatic Write Timing**
  - **$\overline{\text{DATA}}$ Polling and Verification**
  - **Ready/$\overline{\text{Busy}}$ Output Pin**
- **Enhanced Write Protection**
- **Single 5 volt Supply**
- **Byte Write: 10ms (max)—KM2865A**
  2ms (max)—KM2865AH
- **Fast Access Time: 200ns**
- **Power: 50mA—Standby (max)**
  120mA—Operating (max)
- **Two Line Control-Eliminates Bus Contention**
- **10,000 Cycle Endurance**
- **JEDEC Byte-wide Memory Pinout**

GENERAL DESCRIPTION

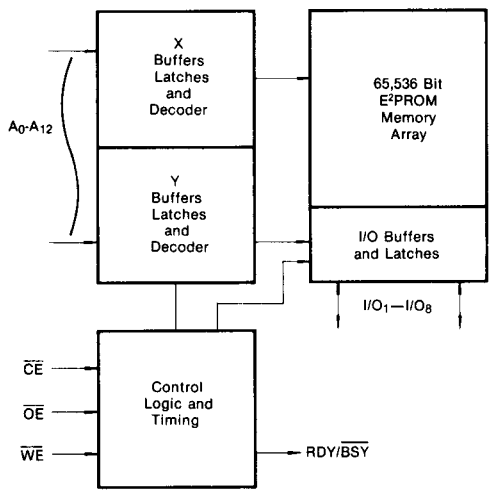
The KM2865A/AH is a 65,536 bit Electrically Erasable and Programmable Read-Only-Memory organized as 8,192 words by 8-bits. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

Writing data into the KM2865A/AH is very simple. The internally self-timed write cycle latches both address and data to provide a free system bus during the write period which is 10ms (max) for the KM2865A or 2ms (max) for the KM2865AH.

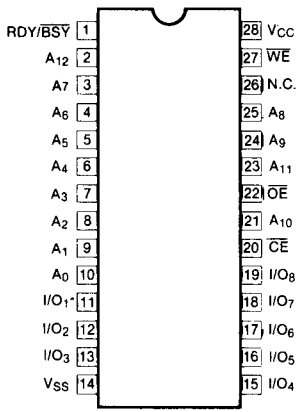
The KM2865A/AH features two end of write detection schemes to provide maximum design flexibility while enhancing the system performance. $\overline{\text{DATA}}$ Polling is a software scheme to detect the early completion of a write cycle without using any additional hardware. Ready/$\overline{\text{Busy}}$ is a hardware scheme in which Pin 1 is used to signal the status of the write operation and is especially useful in interrupt driven systems.

The KM2865A/AH is fabricated with the well defined floating gate NMOS technology using Fowler-Nordheim tunneling for erasing and programming.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{12}	Address Inputs
I/O_1—I/O_8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BSY}$	Ready/$\overline{Busy}$ Output
N.C.	No Connection
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}	−1 to +6.0	V
Temperature Under Bias	T_{bias}	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Short Circuit Output Current	I_{OS}	5	mA

*NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS

(Voltages referenced to V_{SS}, $T_A = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	−1	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Max	Units
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$ All I/O's = OPEN Other Inputs = V_{CC}	—	120	mA
Standby Current	I_{SB}	$\overline{CE} = V_{IH}$ All I/O's = OPEN Other Inputs = V_{CC}	—	50	mA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to 5.5V	—	10	μA
Output High Voltage Level	V_{OH}	$I_{OH} = -400$ μA	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1$ mA	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.5	—	V

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, $f = 1.0$ MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	10	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

($T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0 to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and $C_L = 100$ pF

READ CYCLE

Parameter	Symbol	KM2865A-20 KM2865AH-20		KM2865A-25 KM2865AH-25		KM2865A-30 KM2865AH-30		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200		250		300		ns
Chip Enable Access Time	t_{CE}		200		250		300	ns
Address Access Time	t_{AA}		200		250		300	ns
Output Enable Access Time	t_{OE}		100		120		150	ns
Chip Enable to Output in Low-Z	t_{LZ}	10		10		10		ns
Chip Disable to Output in High-Z	t_{HZ}	10	100	10	100	10	100	ns
Output Enable to Output in Low-Z	t_{OLZ}	50		50		50		ns
Output Disable to Output in High-Z	t_{OHZ}	10	60	10	80	10	100	ns
Output Hold from Address Change	t_{OH}	20		20		20		ns

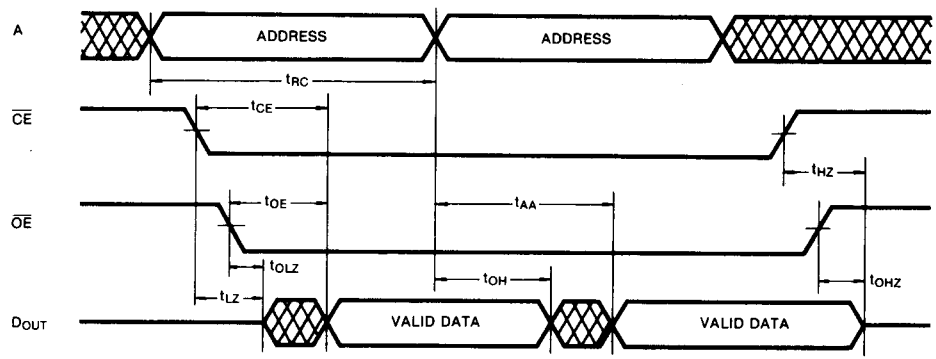
WRITE CYCLE

Parameter		Symbol	Min	Max	Units
Write Cycle Time	KM2865A	t_{WC}	10		ms
	KM2865AH		2		
Address Set-up Time		t_{AS}	10		ns
Address Hold Time		t_{AH}	120		ns
Write Set-up Time		t_{CS}	0		ns
Write Hold Time		t_{CH}	0		ns
Chip Enable to End of Write Input		t_{CW}	150		ns
Output Enable Set-up Time		t_{OES}	10		ns
Output Enable Hold Time		t_{OEH}	10		ns
Write Pulse Width		t_{WP}	150		ns
Data Latch Time		t_{DL}	50		ns
Data Valid Time		t_{DV}		1	μs
Data Set-up Time		t_{DS}	50		ns
Data Hold Time		t_{DH}	10		ns
Time to Device Busy		t_{DB}		120	ns
Busy to Write Recovery Time		t_{BWR}	50		ns

TIMING DIAGRAMS

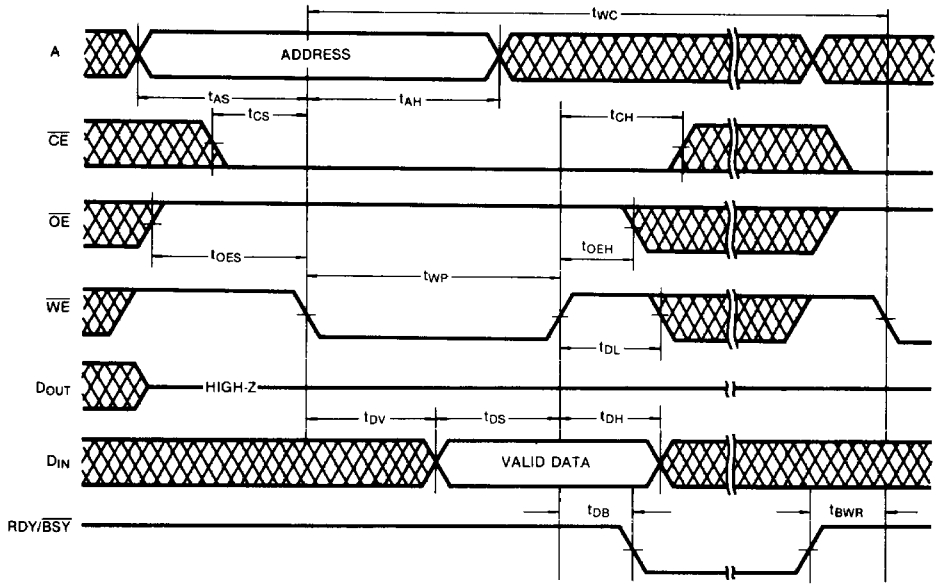
READ CYCLE

$\overline{WE} = V_{IH}$

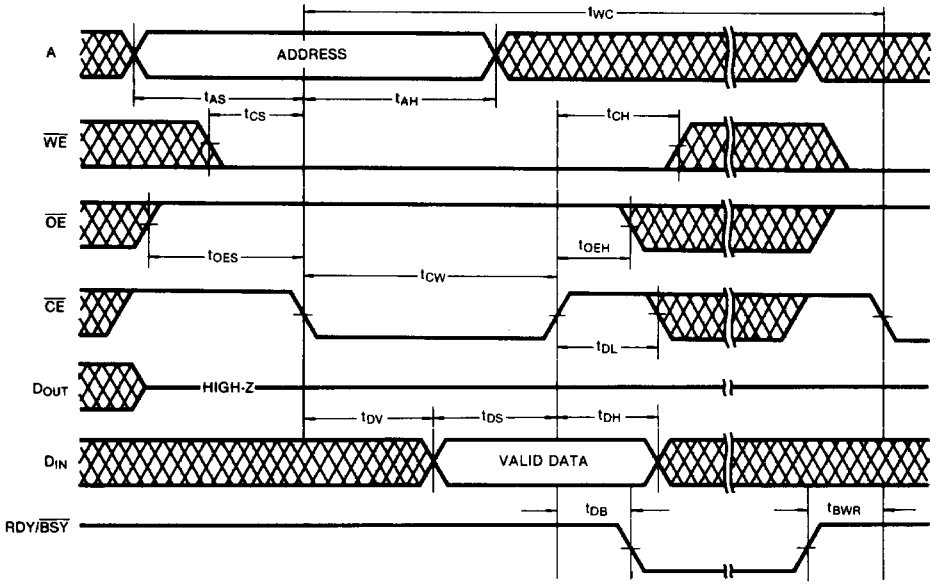


TIMING DIAGRAMS (Continued)

$\overline{WE}$ CONTROLLED WRITE CYCLE



$\overline{CE}$ CONTROLLED WRITE CYCLE



DEVICE OPERATION

Read

Reading data from the KM2865A/AH is similar to reading data from a static RAM. A reading cycle occurs when $\overline{WE}$ is high and both $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high,the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

Write

Writing Data into the KM2865A/AH is very easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a static RAM.
A write cycle occurs when $\overline{OE}$ is high and both $\overline{CE}$ and $\overline{WE}$ are low. The address is latched by the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first. Address and data are conveniently latched in less than 200ns during a write operation. Once a byte write cycle is initiated it will automatically continue to completion within 10ms (max) for the KM2865A or 2ms (max) for the KM2865AH. The existing data at the selected address is automatically erased and the new data is automatically written.

Standby

Power consumption may be reduced about 60% by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and $I/O_1 - I/O_8$ are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

Data Protection

Features have been designed into the KM2865A/AH that prevent unwanted write cycles during power supply transitions and system noise periods.

Write cycles are inhibited when V_{CC} is less than $V_{WI} = 3.5$ volts, the Write Inhibit V_{CC} level.

During power-up the KM2865A/AH automatically prevents any write operaion for a period of 9ms for the KM2865A or 2ms for the KM2865AH after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ or $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period.

Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit inadvertent writes.

$\overline{\text{Data}}$ Polling

The KM2865A/AH features $\overline{DATA}$ Polling to detect the completion of a write cycle using a simple read and compare operation. Such a scheme does not required any external hardware. During a write cycle the most significant bit of the byte written to the KM2865A/AH is inverted and routed to the output buffer. The I/O pins, I/O_1-I/O_7, remain in a high impedance state until a read command is initiated. Reading the device during the write operation will produce this inverted bit at I/O_8 (I/O_1-I/O_7 are indeterminate). True data will be produced at I/O_8 once the write cycle has been completed.

Ready/$\overline{\text{Busy}}$

The KM2865AH has a Ready/$\overline{Busy}$ output pin that indicates when the write cycle is complete. The pin is normally high except when a write cycle is in progress, in which case the pin is low.
The Ready/$\overline{Busy}$ output is configured as open-drain driver there-by allowing two or more Ready/$\overline{Busy}$ output to be or-tied. This pin requires an appropriate pull-up register for proper operation. The pull-up resistor value for the Ready/$\overline{Busy}$ output maybe calculated as follows:

$$R_p = \frac{V_{CC}\,(MAX) - V_{OL}\,(MAX)}{I_{OL} + I_L} = \frac{5.1V}{2.1mA + I_L}$$

Where I_L is the sum of the input currents of all devices tied to the Ready/$\overline{Busy}$ pin.

Endurance and Data Retention

The KM2865A/AH is designed for applications requiring, up to 10,000 write cycles per E^2PROM byte and ten years of data retention. This means that each byte may be reliably written 10,000 times without degrading device operation, and that the data in the byte will remain valid after its last rewrite operation for ten years with or without power applied.

PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)