

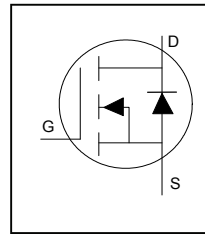
Application

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

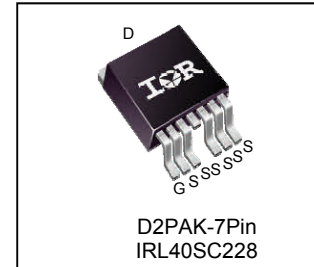
Benefits

- Optimized for Logic Level Drive
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free*
- RoHS Compliant, Halogen-Free

HEXFET® Power MOSFET



V_{DSS}	40V
R_{DS(on)} typ.	0.50mΩ
max	0.65mΩ
I_D (Silicon Limited)	557A①
I_D (Package Limited)	360A



G	D	S
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRL40SC228	D2PAK-7Pin	Tape and Reel Left	800	IRL40SC228

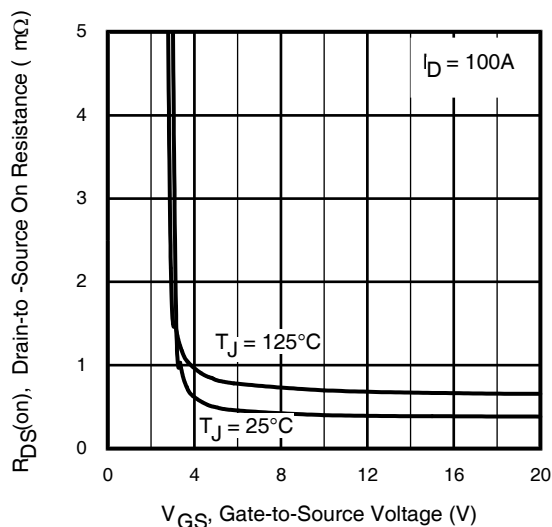


Fig 1. Typical On-Resistance vs. Gate Voltage

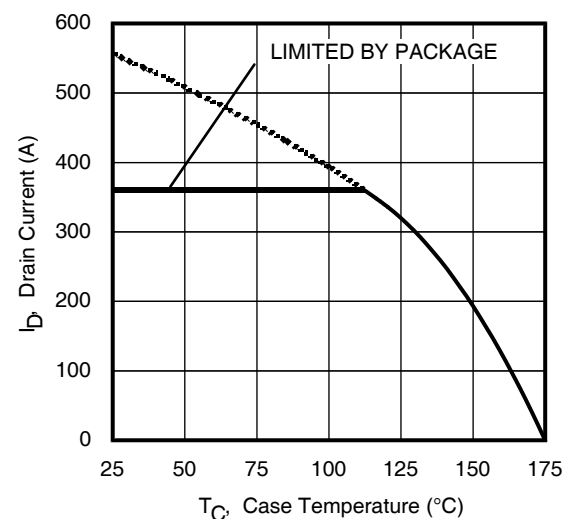


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	557 ^①	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	393 ^①	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Wire Bond Limited)	360	
I_{DM}	Pulsed Drain Current ^②	1440 ^⑩	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	416	W
	Linear Derating Factor	2.8	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J	Operating Junction and	-55 to + 175	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ^③	1275	mJ
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ^⑨	2150	
I_{AR}	Avalanche Current ^②	See Fig 15, 16, 23a, 23b	A
E_{AR}	Repetitive Avalanche Energy ^②		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ^⑧	—	0.36	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient *	—	62	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.031	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 5\text{mA}$ ^②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.50	0.65	m Ω	$V_{GS} = 10\text{V}$, $I_D = 100\text{A}$ ^⑤
		—	0.60	0.90		$V_{GS} = 4.5\text{V}$, $I_D = 50\text{A}$ ^⑤
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.4	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 40\text{V}$, $V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 40\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
R_G	Gate Resistance	—	2.2	—	Ω	

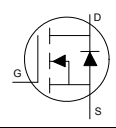
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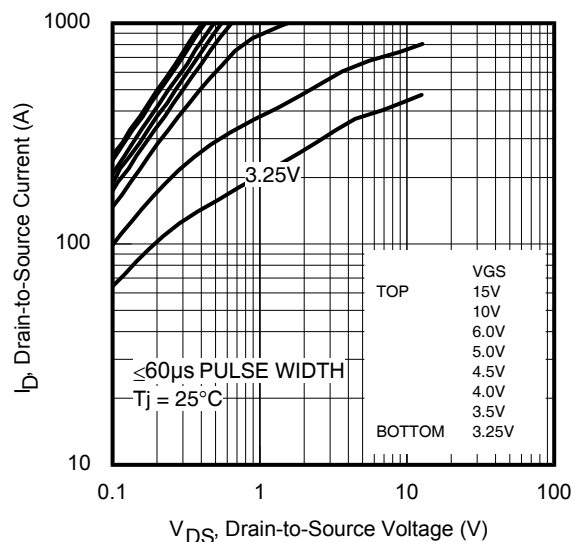
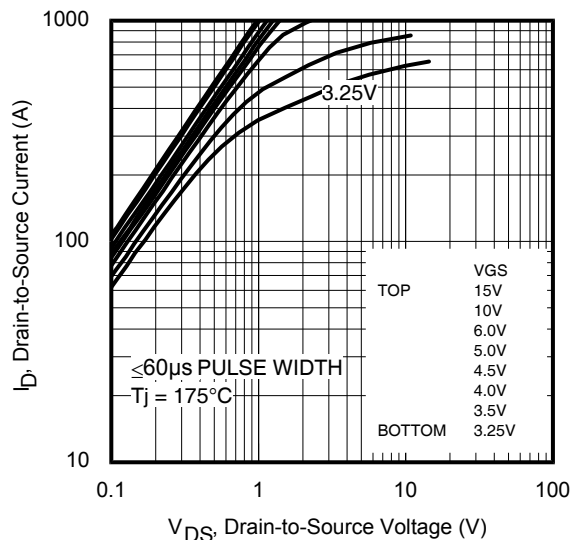
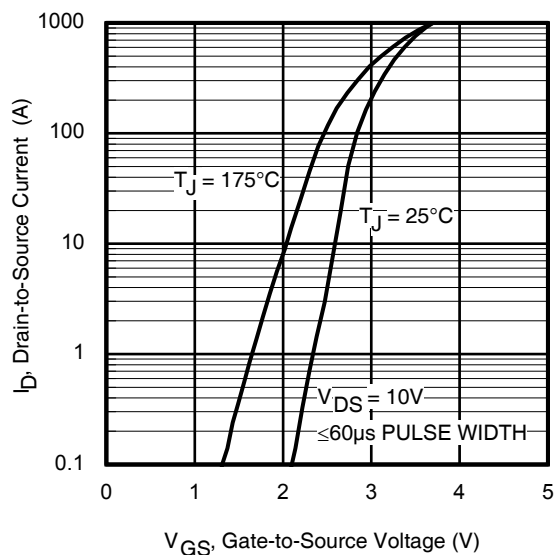
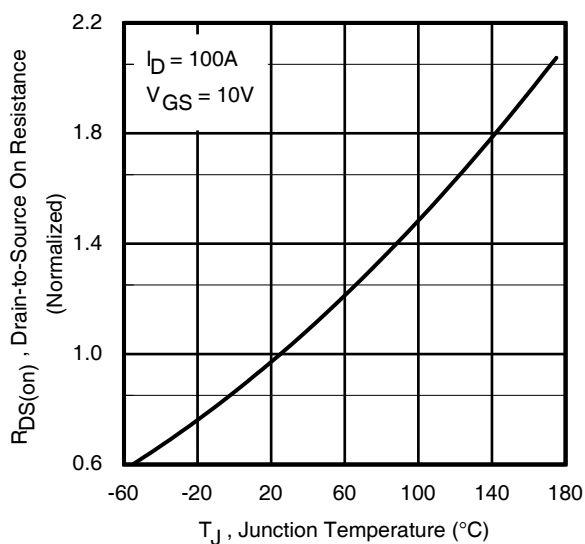
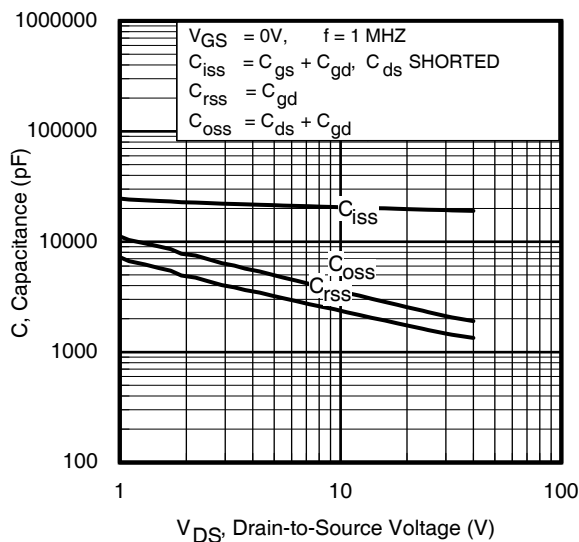
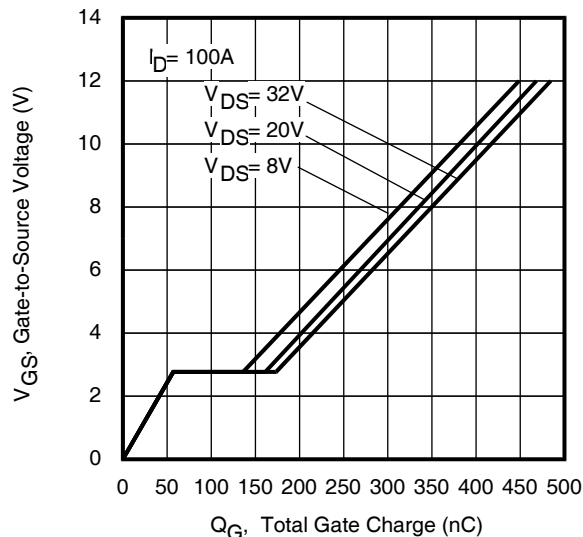
- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 360A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
 - ② Repetitive rating; pulse width limited by max. junction temperature.
 - ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.146\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 100\text{A}$, $V_{GS} = 10\text{V}$.
 - ④ $I_{SD} \leq 100\text{A}$, $di/dt \leq 1008\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
 - ⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
 - ⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
 - ⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
 - ⑧ R_θ is measured at T_J approximately 90°C .
 - ⑨ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 1\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 65\text{A}$, $V_{GS} = 10\text{V}$.
 - ⑩ Pulse drain current is limited to 1440A by source bonding technology.
- * When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994: <http://www.infineon.com/technical-info/appnotes/an-994.pdf>

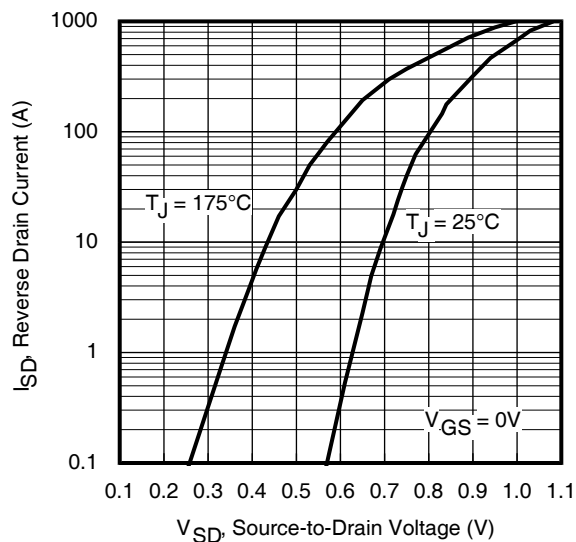
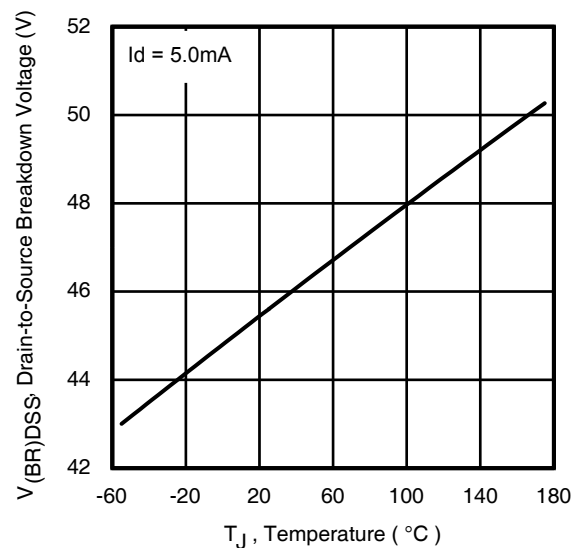
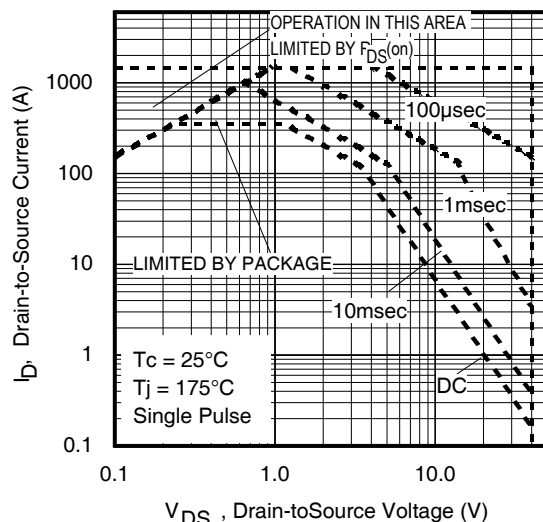
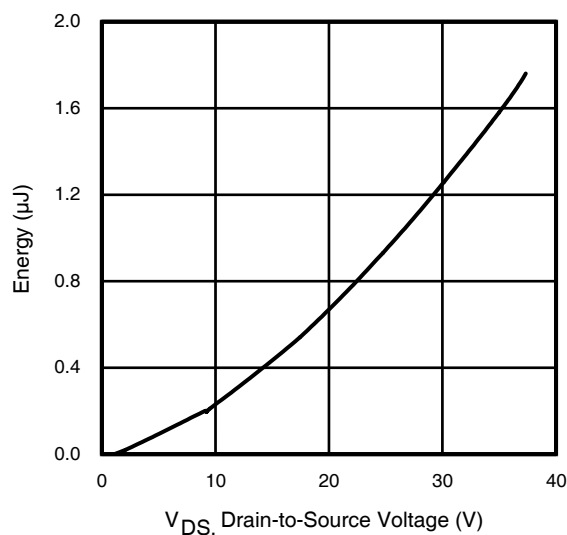
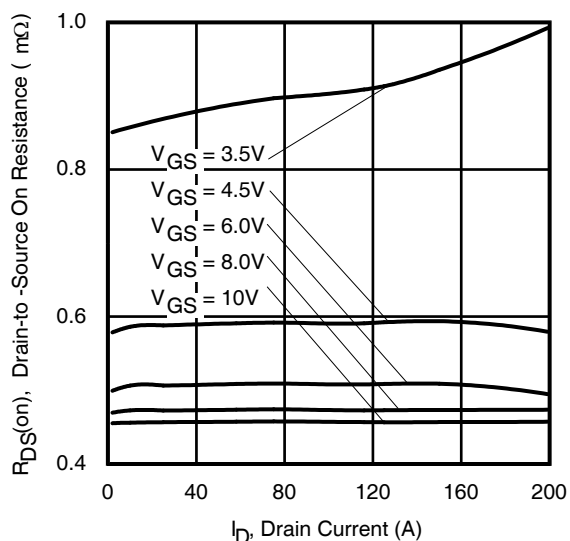
Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

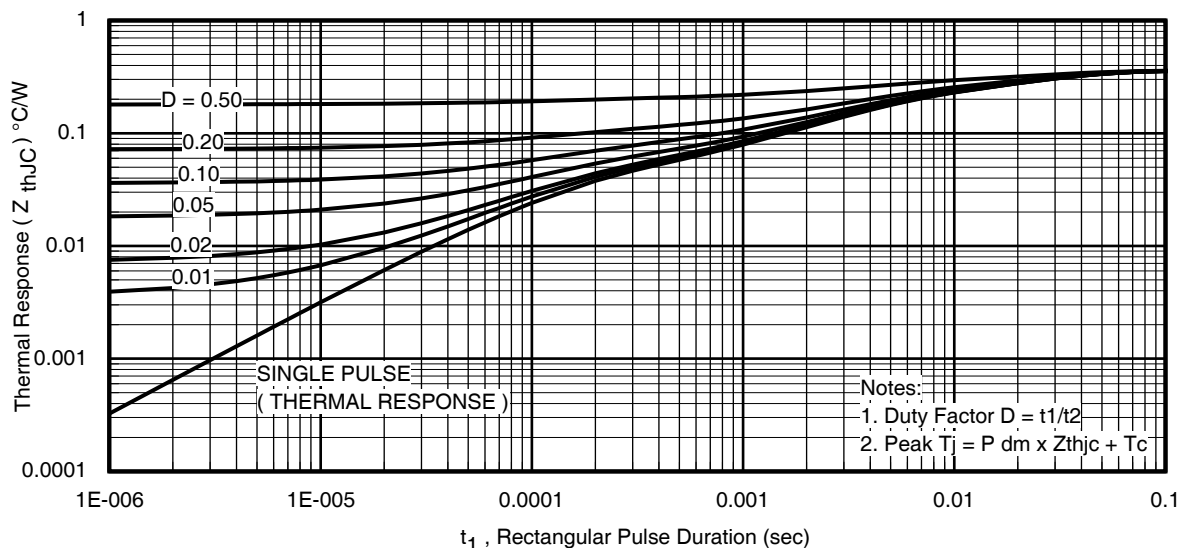
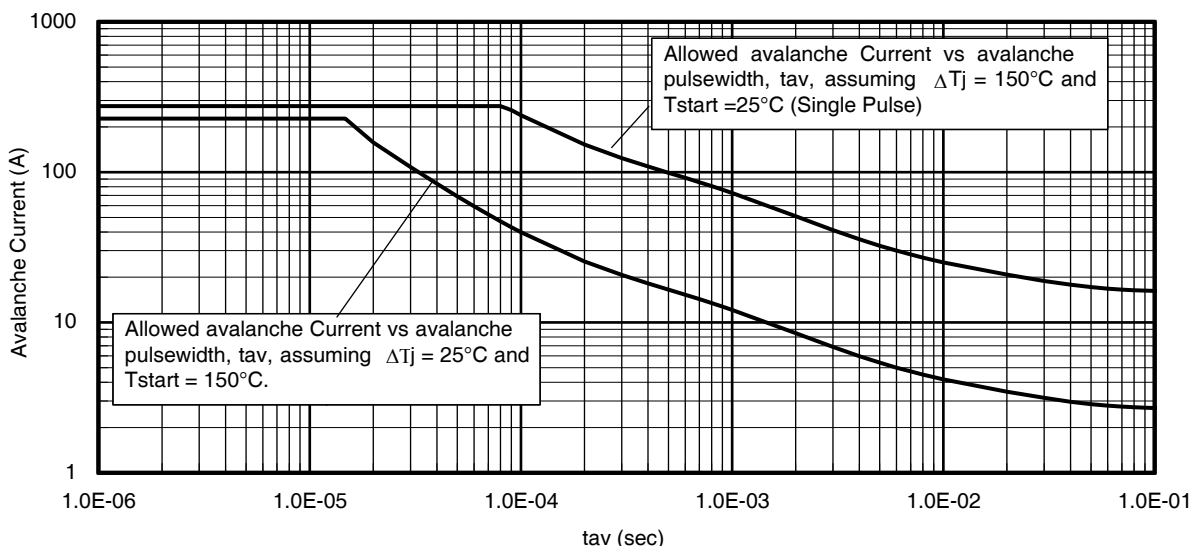
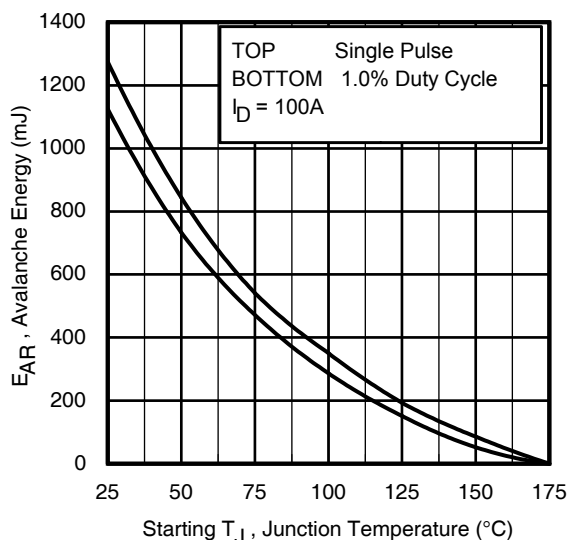
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	264	—	—	S	$V_{DS} = 10\text{V}$, $I_D = 100\text{A}$
Q_g	Total Gate Charge	—	205	307	nC	$I_D = 100\text{A}$ $V_{DS} = 20\text{V}$ $V_{GS} = 4.5\text{V}^{(5)}$
Q_{gs}	Gate-to-Source Charge	—	57	—		
Q_{gd}	Gate-to-Drain Charge	—	104	—		
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	101	—		
$t_{d(on)}$	Turn-On Delay Time	—	67	—	ns	$V_{DD} = 20\text{V}$ $I_D = 30\text{A}$ $R_G = 2.7\Omega$ $V_{GS} = 4.5\text{V}^{(5)}$
t_r	Rise Time	—	210	—		
$t_{d(off)}$	Turn-Off Delay Time	—	222	—		
t_f	Fall Time	—	176	—		
C_{iss}	Input Capacitance	—	19680	—	pF	$V_{GS} = 0\text{V}$ $V_{DS} = 25\text{V}$ $f = 1.0\text{MHz}$, See Fig.7
C_{oss}	Output Capacitance	—	2305	—		$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$ to $32\text{V}^{(7)}$
C_{rss}	Reverse Transfer Capacitance	—	1575	—		$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$ to $32\text{V}^{(6)}$
$C_{oss\text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	2690	—		
$C_{oss\text{ eff. (TR)}}$	Output Capacitance (Time Related)	—	3390	—		

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	557 ⁽¹⁾	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ⁽²⁾	—	—	1440 ⁽¹⁰⁾		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}$, $I_S = 100\text{A}$, $V_{GS} = 0\text{V}$ ⁽⁵⁾
dv/dt	Peak Diode Recovery dv/dt ⁽⁴⁾	—	2.0	—	V/ns	$T_J = 175^\circ\text{C}$, $I_S = 100\text{A}$, $V_{DS} = 40\text{V}$
t_{rr}	Reverse Recovery Time	—	42 43	—	ns	$T_J = 25^\circ\text{C}$ $V_{DD} = 34\text{V}$ $T_J = 125^\circ\text{C}$ $I_F = 100\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$ ⁽⁵⁾
Q_{rr}	Reverse Recovery Charge	—	43 45	—		
I_{RRM}	Reverse Recovery Current	—	1.7	—	A	$T_J = 25^\circ\text{C}$

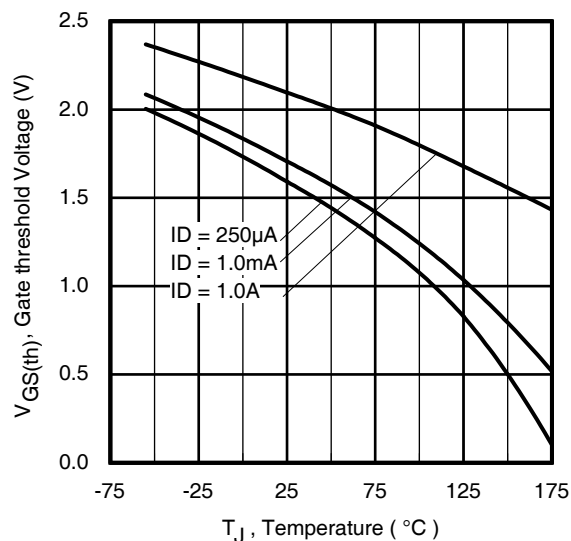
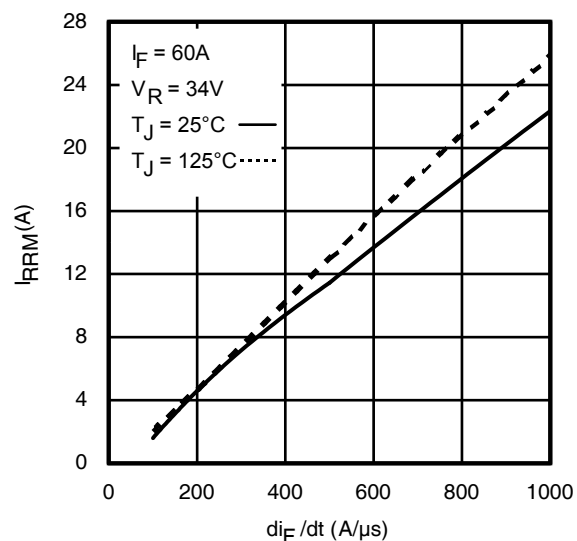
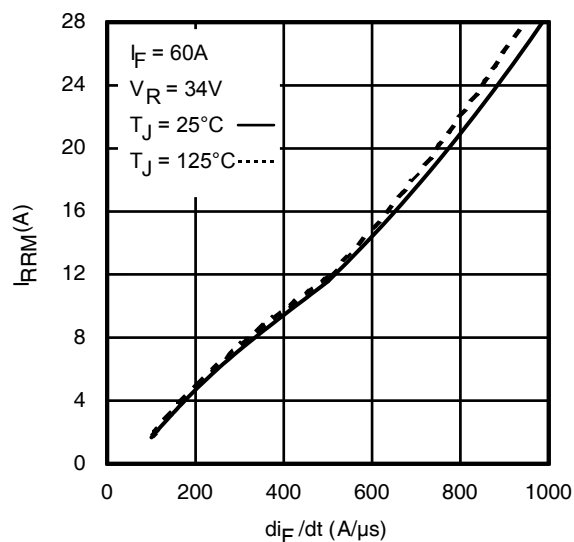
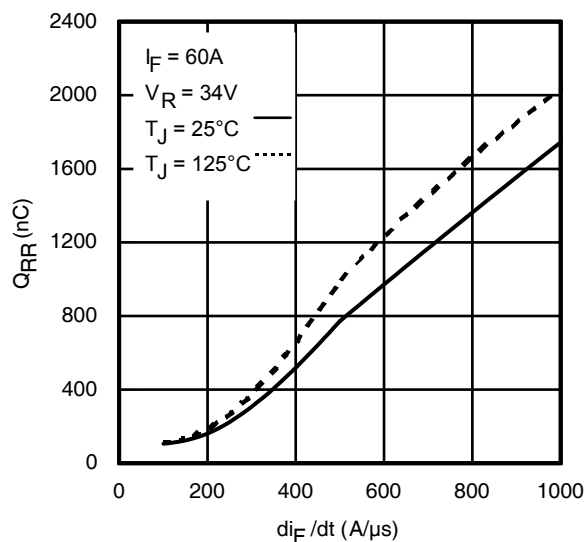
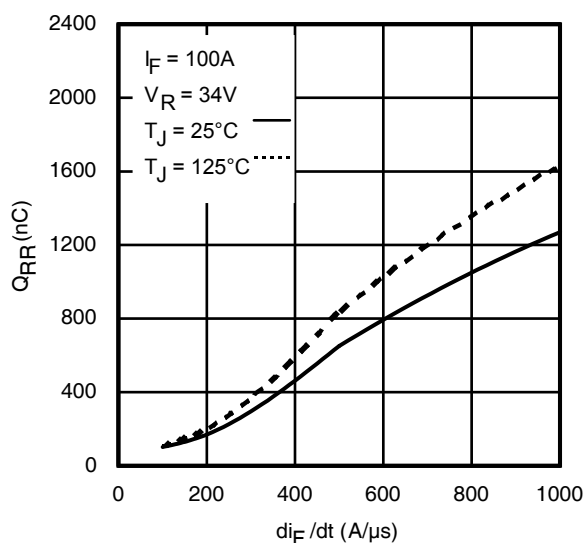

Fig 3. Typical Output Characteristics

Fig 4. Typical Output Characteristics

Fig 5. Typical Transfer Characteristics

Fig 6. Normalized On-Resistance vs. Temperature

Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 9. Typical Source-Drain Diode Forward Voltage

Fig 11. Drain-to-Source Breakdown Voltage

Fig 10. Maximum Safe Operating Area

Fig 12. Typical C_{OSS} Stored Energy

Fig 13. Typical On-Resistance vs. Drain Current


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 15. Avalanche Current vs. Pulse Width

Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 14)
 $P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$


Fig 17. Threshold Voltage vs. Temperature

Fig 18. Typical Recovery Current vs. di_F/dt

Fig 19. Typical Recovery Current vs. di_F/dt

Fig 20. Typical Stored Charge vs. di_F/dt

Fig 21. Typical Stored Charge vs. di_F/dt

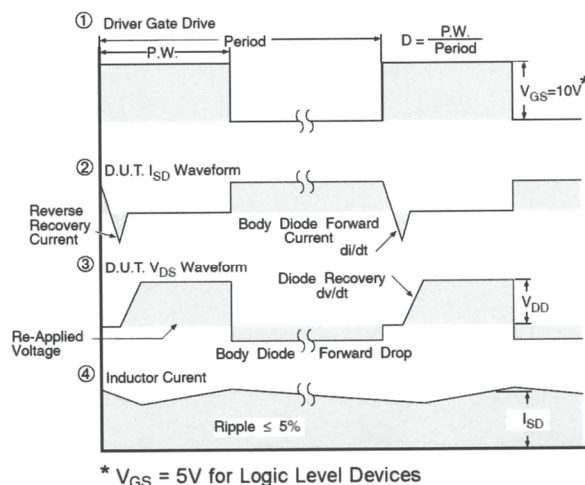
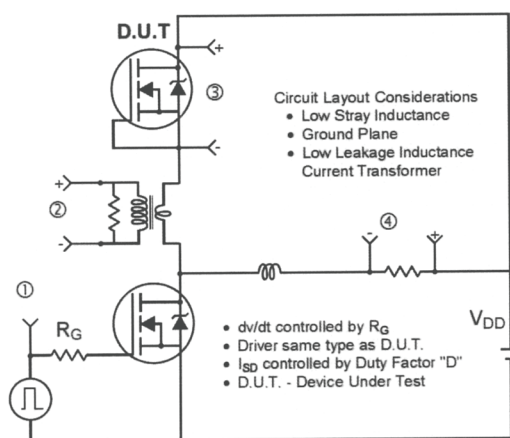


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

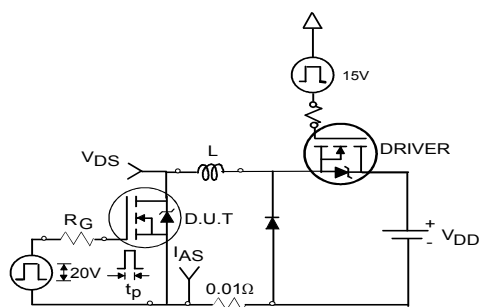


Fig 23a. Unclamped Inductive Test Circuit

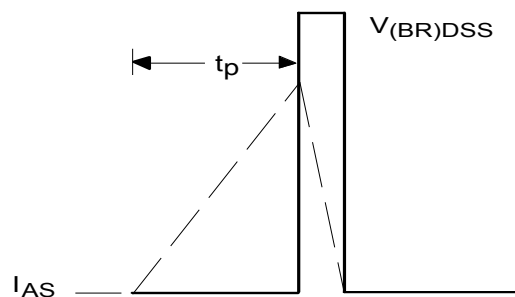


Fig 23b. Unclamped Inductive Waveforms

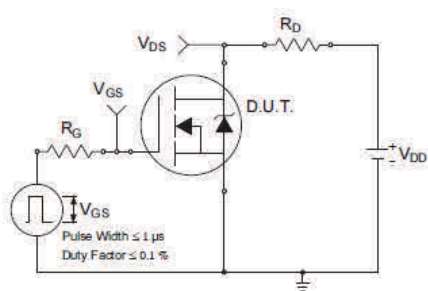


Fig 24a. Switching Time Test Circuit

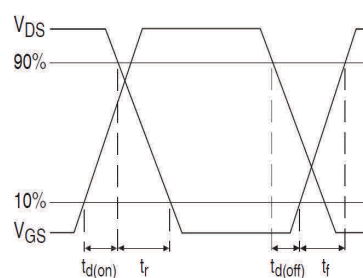


Fig 24b. Switching Time Waveforms

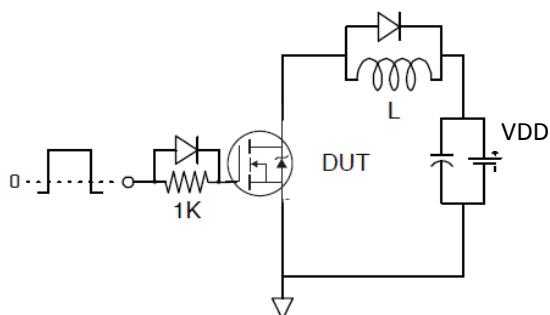


Fig 25a. Gate Charge Test Circuit

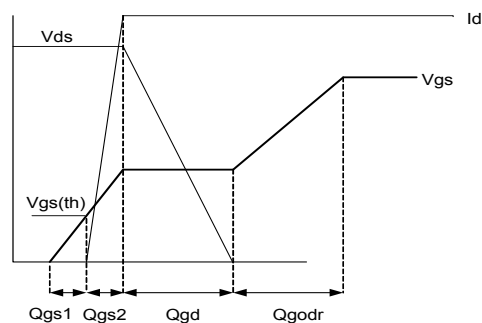
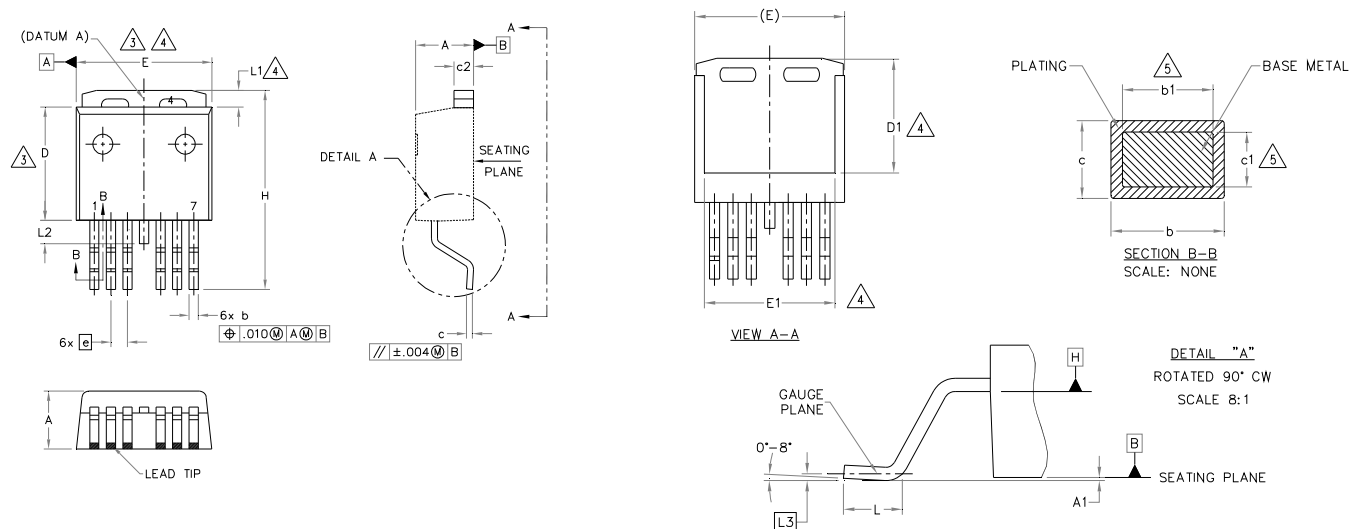


Fig 25b. Gate Charge Waveform

D²Pak - 7 Pin Package Outline (Dimensions are shown in millimeters (inches))

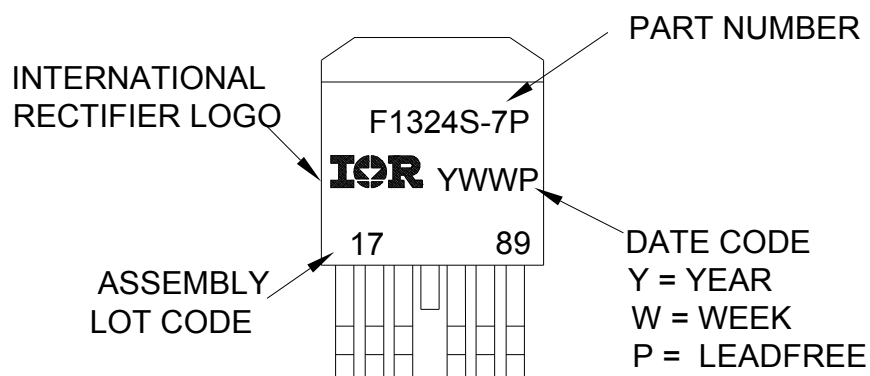


SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	—	0.254	—	.010	
b	0.51	0.91	.020	.036	
b1	0.51	0.81	.020	.032	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	4
D	8.38	9.65	.330	.380	
D1	6.86	7.42	.270	.292	
E	9.65	10.54	.380	.415	
E1	8.00	9.00	.315	.354	
e	1.27 BSC		.050 BSC		4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		

NOTES:

- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994
- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
- DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- CONTROLLING DIMENSION: INCH.
- OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB. EXCEPT FOR DIMS. E, E1 & D1.

D²Pak - 7 Pin Part Marking Information



Qualification Information

Qualification Level	Industrial (per JEDEC JESD47F) [†]	
Moisture Sensitivity Level	D2PAK-7Pin	MSL1 (per JEDEC J-STD-020D [†])
RoHS Compliant	Yes	

[†] Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
05/12/2017	Corrected package picture added "s" on pin number 4 - page 1.

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