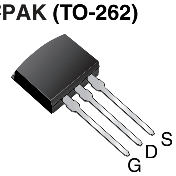
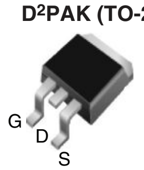
# Power MOSFET

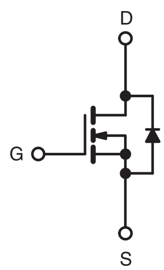
| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | 400 | |
| $R_{DS(on)}$ (Ω) | $V_{GS}$ = 10 V | 0.55 |
| $Q_g$ (Max.) (nC) | 36 | |
| $Q_{gs}$ (nC) | 9.9 | |
| $Q_{gd}$ (nC) | 16 | |
| Configuration | Single | |

I2PAK (TO-262)




D2PAK (TO-263)




N-Channel MOSFET

## FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- Low Gate Charge $Q_g$ Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective $C_{oss}$ specified
- Compliant to RoHS Directive 2002/95/EC

Pb Available
RoHS* COMPLIANT
HALOGEN FREE Available

## APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High speed Power Switching

## TYPICAL SMPS TOPOLOGIES

- Single Transistor Flyback Xfmr. Reset
- Single Transistor Forward Xfmr. Reset (Both for US Line Input Only)

| ORDERING INFORMATION | | | | |
|---|---|---|---|---|
| Package | D2PAK (TO-263) | D2PAK (TO-263) | D2PAK (TO-263) | I2PAK (TO-262) |
| Lead (Pb)-free and Halogen-free | SiHF740AS-GE3 | SiHF740ASTRL-GE3[a] | SiHF740ASTRR-GE3[a] | SiHF740AL-GE3 |
| Lead (Pb)-free | IRF740ASPbF | IRF740ASTRLPbF[a] | IRF740ASTRRPbF[a] | IRF740ALPbF |
| | SiHF740AS-E3 | SiHF740ASTL-E3[a] | SiHF740ASTR-E3[a] | SiHF740AL-E3 |
| SnPb | IRF740AS | IRF740ASTRL[a] | IRF740ASTRR[a] | IRF740AL |
| | SiHF740AS | SiHF740ASTL[a] | SiHF740ASTR[a] | SiHF740AL |

**Note**
a. See device orientation.

**ABSOLUTE MAXIMUM RATINGS** ($T_C$ = 25 °C, unless otherwise noted)

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|---|
| Drain-Source Voltage | | | $V_{DS}$ | 400 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 30 | |
| Continuous Drain Current[e] | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 10 | A |
| | | $T_C$ = 100 °C | | 6.3 | |
| Pulsed Drain Current[a, e] | | | $I_{DM}$ | 40 | |
| Linear Derating Factor | | | | 1.0 | W/°C |
| Single Pulse Avalanche Energy[b, e] | | | $E_{AS}$ | 630 | mJ |
| Avalanche Current[a] | | | $I_{AR}$ | 10 | A |
| Repetiitive Avalanche Energy[a] | | | $E_{AR}$ | 12.5 | mJ |
| Maximum Power Dissipation | $T_A$ = 25 °C | | $P_D$ | 3.1 | W |
| | $T_C$ = 25 °C | | | 125 | |
| Peak Diode Recovery dV/dt[c, e] | | | dV/dt | 5.9 | V/ns |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | - 55 to + 150 | °C |
| Soldering Recommendations (Peak Temperature) | for 10 s | | | 300[d] | |

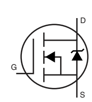
**Notes**
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Starting $T_J$ = 25 °C, L = 12.6 mH, $R_g$ = 25 Ω, $I_{AS}$ = 10 A (see fig. 12).
c. $I_{SD} \le$ 10 A, dI/dt ≤ 330 A/μs, $V_{DD} \le V_{DS}$, $T_J \le$ 150 °C.
d. 1.6 mm from case.
e. Uses IRF740A, SiHF740A data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply

| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient (PCB Mounted, Steady-State)[a] | $R_{thJA}$ | - | 40 | °C/W |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | 1.0 | |

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 400 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA[d] | - | 0.48 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D$ = 250 µA | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 30 V | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V | - | - | 25 | µA |
| | | $V_{DS}$ = 320 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V; $I_D$ = 6.0 A[b] | - | - | 0.55 | Ω |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 50 V, $I_D$ = 6.0 A[d] | 4.9 | - | - | S |
| **Dynamic** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1.0 MHz, see fig. 5[d] | - | 1030 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 170 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 7.7 | - | |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V; $V_{DS}$ = 1.0 V, f = 1.0 MHz | - | 1490 | - | |
| | | $V_{GS}$ = 0 V; $V_{DS}$ = 320 V, f = 1.0 MHz | - | 52 | - | |
| Effective Output Capacitance | $C_{oss}$ eff. | $V_{GS}$ = 0 V; $V_{DS}$ = 0 V to 320 V[c, d] | - | 61 | - | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = 10 V; $I_D$ = 10 A, $V_{DS}$ = 320 V, see fig. 6 and 13[b, d] | - | - | 36 | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | - | 9.9 | |
| Gate-Drain Charge | $Q_{gd}$ | | - | - | 16 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 200 V, $I_D$ = 10 A, $R_g$ = 10 Ω, $R_D$ = 19.5 Ω, see fig. 10[b, d] | - | 10 | - | ns |
| Rise Time | $t_r$ | | - | 35 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 24 | - | |
| Fall Time | $t_f$ | | - | 22 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 10 | A |
| Pulsed Diode Forward Current[a] | $I_{SM}$ | | - | - | 40 | |
| Body Diode Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 10 A, $V_{GS}$ = 0 V[b] | - | - | 2.0 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = 10 A, dI/dt = 100 A/µs[b, d] | - | 240 | 360 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | - | 1.9 | 2.9 | µC |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

c. $C_{oss}$ eff. is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80 % $V_{DS}$.

d. Uses IRF740A, SiHF740A data and test conditions.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

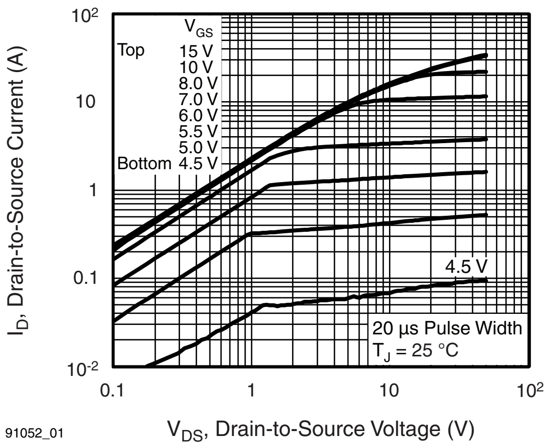



**Fig. 1 - Typical Output Characteristics**

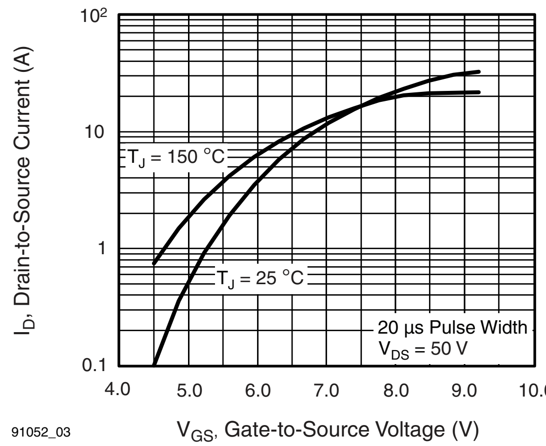



**Fig. 3 - Typical Transfer Characteristics**

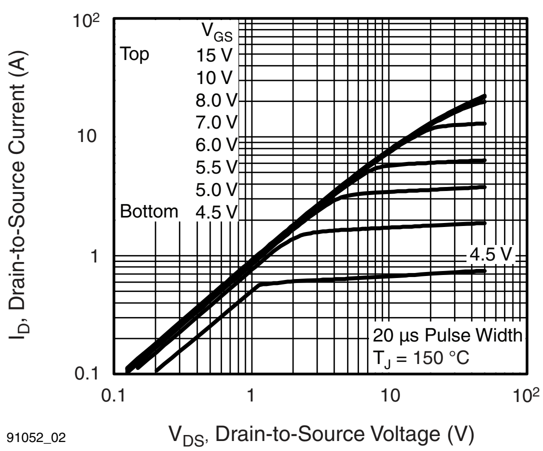



**Fig. 2 - Typical Output Characteristics**

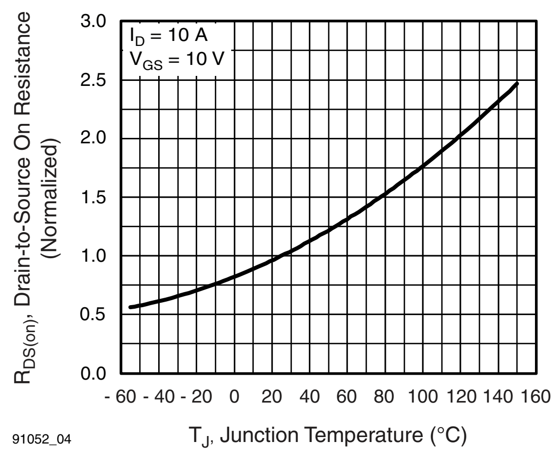



**Fig. 4 - Normalized On-Resistance vs. Temperature**

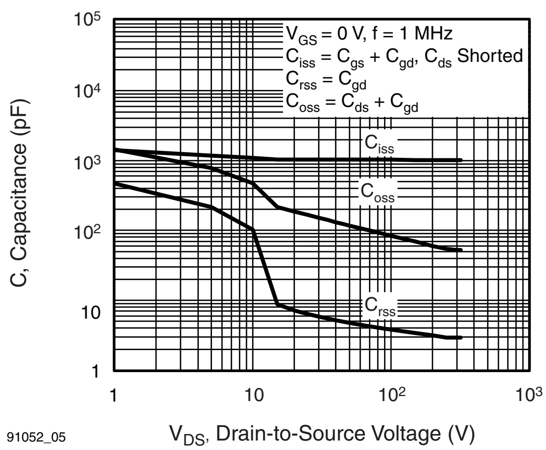



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

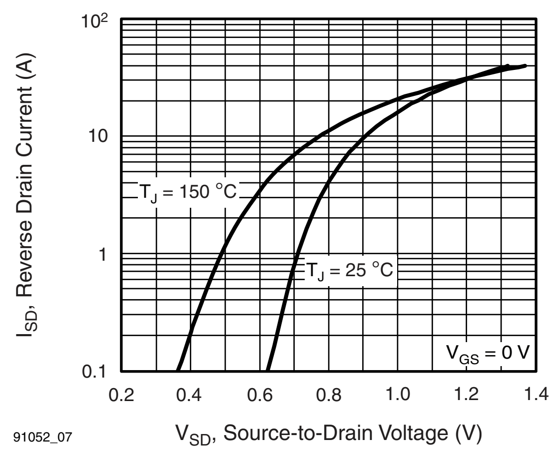



**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

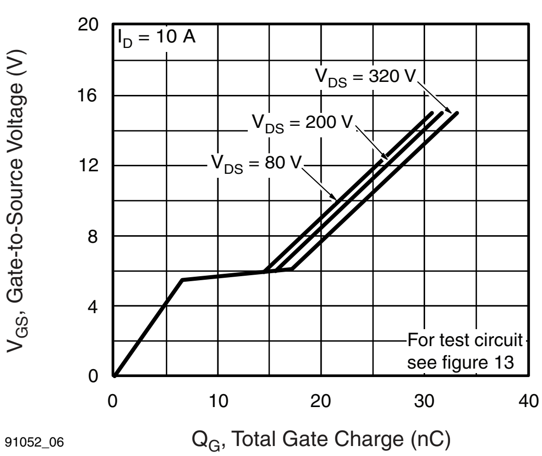



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

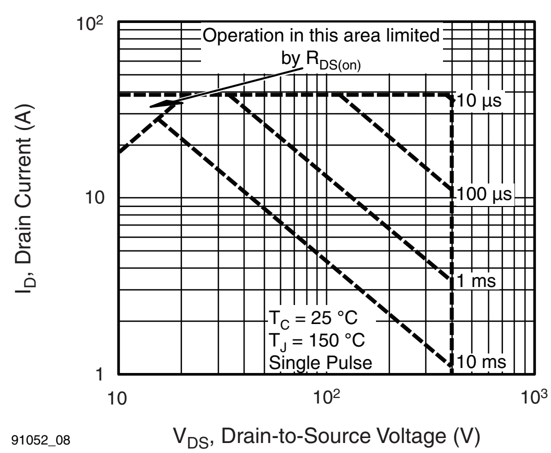



**Fig. 8 - Maximum Safe Operating Area**

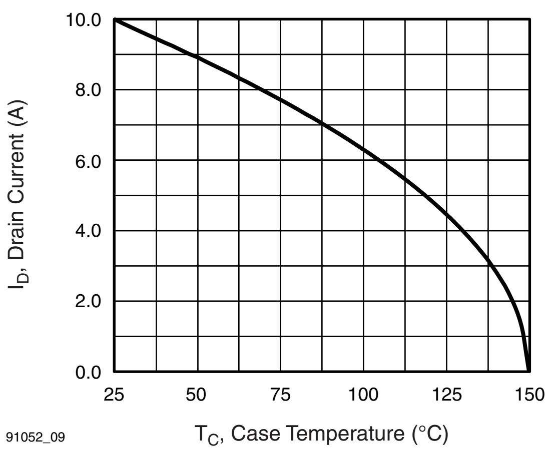



**Fig. 9 - Maximum Drain Current vs. Case Temperature**

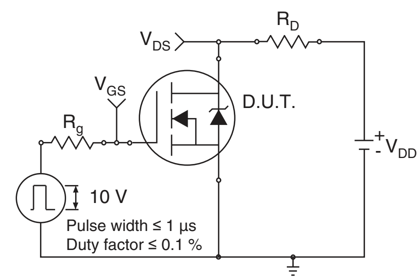



**Fig. 10a - Switching Time Test Circuit**

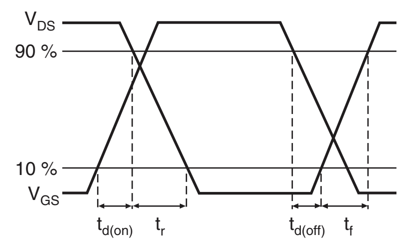



**Fig. 10b - Switching Time Waveforms**

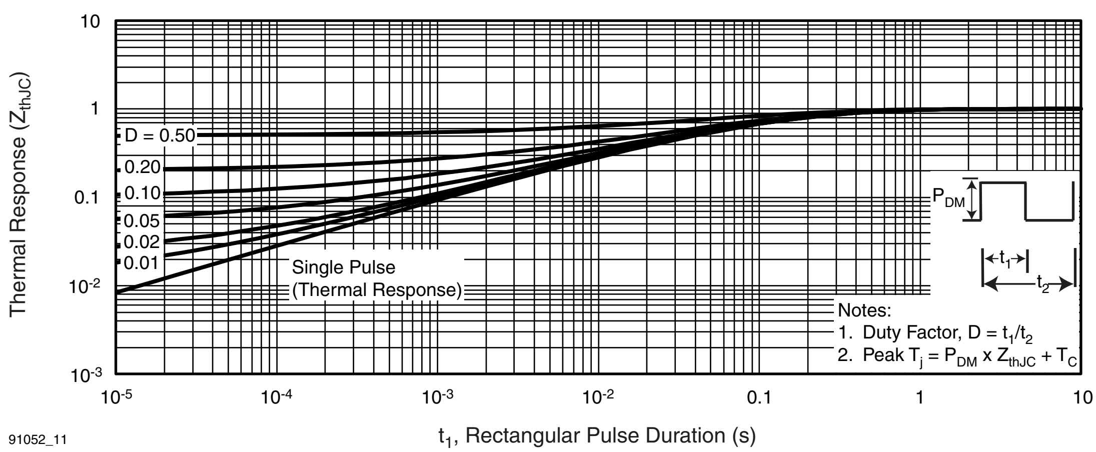



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

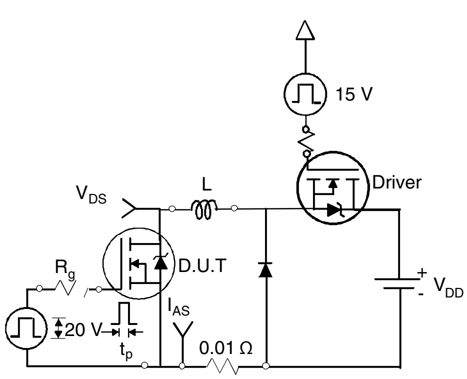



**Fig. 12a - Unclamped Inductive Test Circuit**

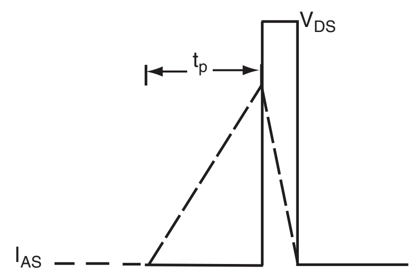



**Fig. 12b - Unclamped Inductive Waveforms**

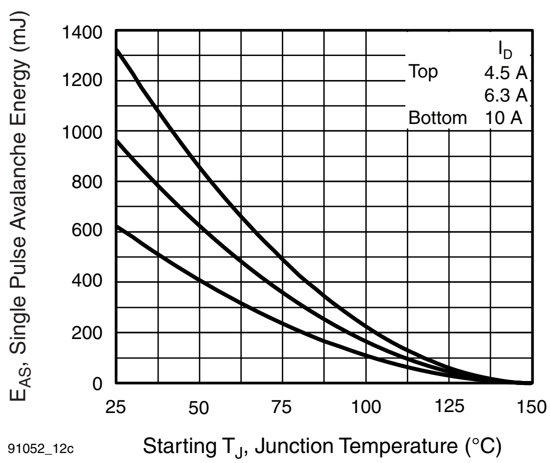



Fig. 12c - Maximum Avalanche Energy vs. Drain Current

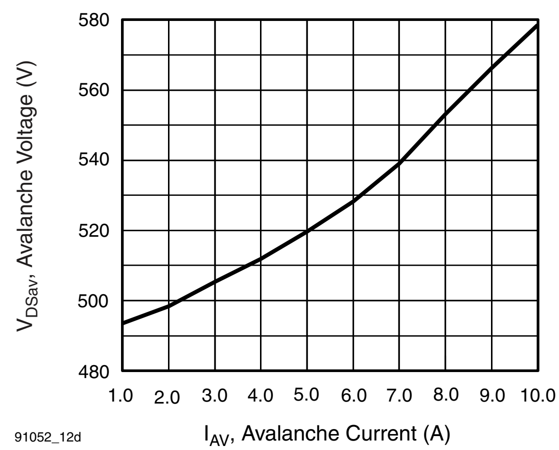



Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

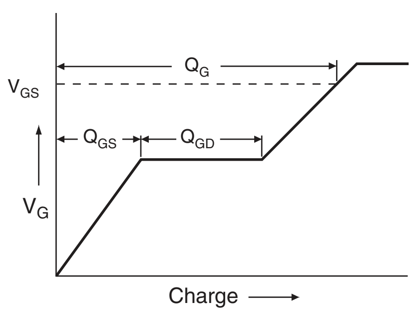



Fig. 13a - Basic Gate Charge Waveform

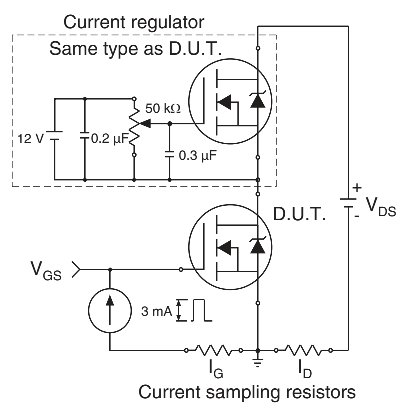
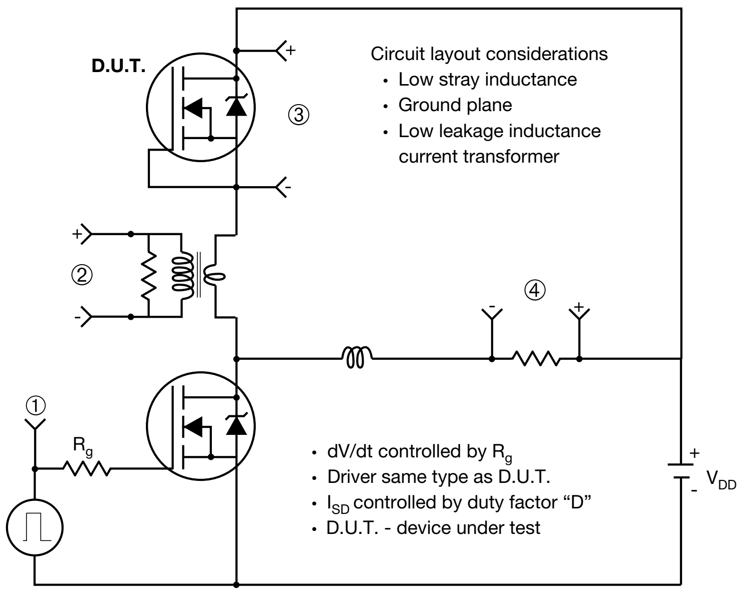
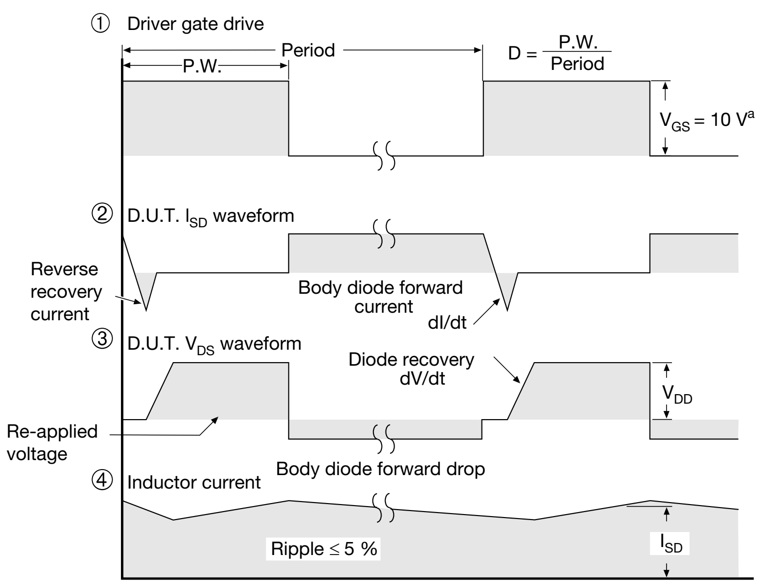



Fig. 13b - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**




**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 14 - For N-Channel**

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