Universal High Brightness LED Driver

Features

- Switch mode controller for single switch LED drivers
- Enhanced drop-in replacement to the HV9910
- Open loop peak current controller
- Internal 8.0 to 450V linear regulator
- Constant frequency or constant off-time operation
- Linear and PWM dimming capability
- Requires few external components for operation

Applications

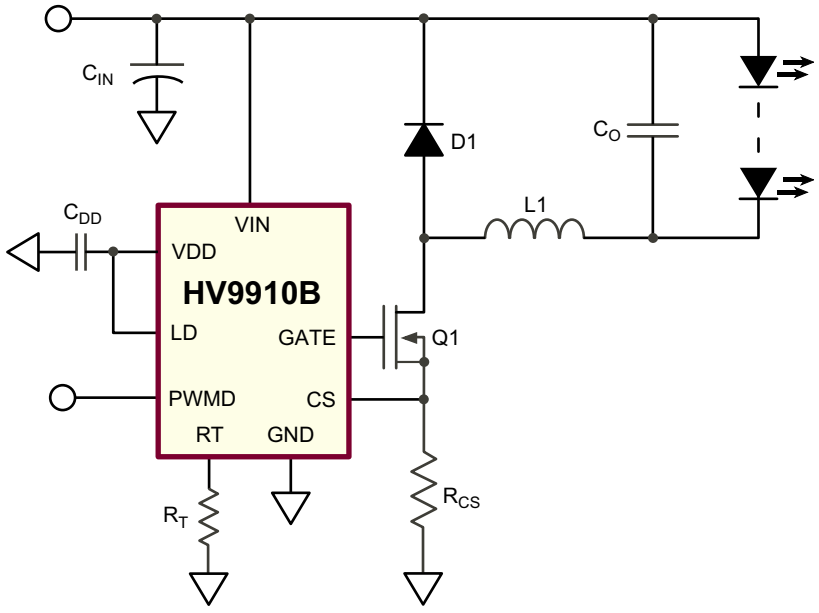
- DC/DC or AC/DC LED driver applications
- RGB backlighting LED driver
- Back lighting of flat panel displays
- General purpose constant current source
- Signage and decorative LED lighting
- Chargers

General Description

The HV9910B is an open loop, current mode, control LED driver IC. The HV9910B can be programmed to operate in either a constant frequency or constant off-time mode. It includes an 8.0 - 450V linear regulator which allows it to work from a wide range of input voltages without the need for an external low voltage supply. The HV9910B includes a PWM dimming input that can accept an external control signal with a duty ratio of 0 - 100% and a frequency of up to a few kilohertz. It also includes a 0 - 250mV linear dimming input which can be used for linear dimming of the LED current.

The HV9910B is ideally suited for buck LED drivers. Since the HV9910B operates in open loop current mode control, the controller achieves good output current regulation without the need for any loop compensation. PWM dimming response is limited only by the rate of rise and fall of the inductor current, enabling very fast rise and fall times. The HV9910B requires only three external components (apart from the power stage) to produce a controlled LED current making it an ideal solution for low cost LED drivers.

Typical Application Circuit

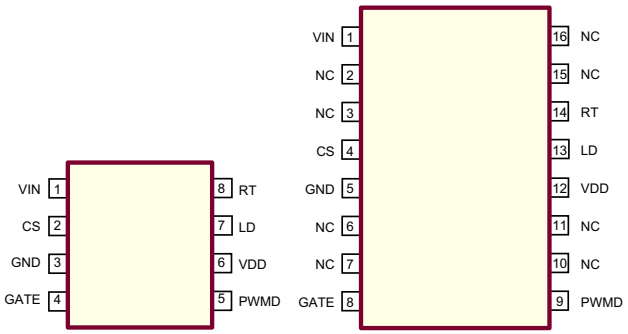


Ordering Information

Device	Package Options	
	8-Lead SOIC	16-Lead SOIC
HV9910B	HV9910BLG-G	HV9910BNG-G

-G indicates package is RoHS compliant ('Green')

Pin Description



8-Lead SOIC (LG) **16-Lead SOIC (NG)**

Absolute Maximum Ratings

Parameter	Value
V_{IN} to GND	-0.5V to +470V
V_{DD} to GND	12V
CS, LD, PWMD, GATE, RT to GND	-0.3V to (V_{DD} +0.3V)
Junction temperature range	-40°C to +150°C
Storage temperature range	-65°C to +150°C
Continuous power dissipation *(T_A = +25°C)* 8-Lead SOIC 16-Lead SOIC	 630mW 1300mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

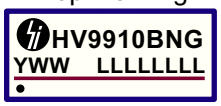
Product Marking

Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

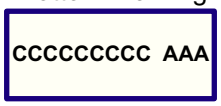
Package may or may not include the following marks: Si or

8-Lead SOIC (LG)

Top Marking



Bottom Marking



Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
_____ = "Green" Packaging
**May be part of top marking*

Package may or may not include the following marks: Si or

16-Lead SOIC (NG)

Thermal Resistance

Package	θ_{ja}
8-Lead SOIC	128°C/W
16-Lead SOIC	82°C/W

Electrical Characteristics *(The specifications are at T_A = 25°C and V_{IN} = 12V, unless otherwise noted.)*

Sym	Description		Min	Typ	Max	Units	Conditions
Input							
V_{INDC}	Input DC supply voltage range[1]	*	8.0	-	450	V	DC input voltage
I_{INSD}	Shut-down mode supply current	*	-	0.5	1.0	mA	Pin PWMD to GND

Notes:

1. *Also limited by package power dissipation limit, whichever is lower.*

† *V_{DD} load current external to the HV9910B.*

* *Denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C.*

\# *Guaranteed by design.*

Electrical Characteristics *(cont.)* *(The specifications are at T_A = 25°C and V_{IN} = 12V, unless otherwise noted.)*

Sym	Description		Min	Typ	Max	Units	Conditions
Internal Regulator							
V_{DD}	Internally regulated voltage	-	7.25	7.5	7.75	V	V_{IN} = 8.0V, $I_{DD(ext)}$ (†) = 0, 500pF at GATE; R_T = 226kΩ, PWMD = V_{DD}
$\Delta V_{DD, line}$	Line regulation of V_{DD}	-	0	-	1.0	V	V_{IN} = 8.0 - 450V, $I_{DD(ext)}$ = 0, 500pF at GATE; R_T = 226kΩ, PWMD = V_{DD}
Internal Regulator							
$\Delta V_{DD, load}$	Load regulation of V_{DD}	-	0	-	100	mV	$I_{DD(ext)}$ = 0 - 1.0mA, 500pF at GATE; R_T = 226kΩ, PWMD = V_{DD}
UVLO	V_{DD} undervoltage lockout threshold	*	6.45	6.7	6.95	V	V_{DD} rising
ΔUVLO	V_{DD} undervoltage lockout hysteresis	-	-	500	-	mV	V_{DD} falling
$I_{IN,MAX}$	Current that the regulator can supply before IC goes into UVLO	#	5.0	-	-	mA	V_{IN} = 8.0V
PWM Dimming							
$V_{EN(lo)}$	Pin PWMD input low voltage	*	-	-	0.8	V	V_{IN} = 8.0 - 450V
$V_{EN(hi)}$	Pin PWMD input high voltage	*	2.0	-	-	V	V_{IN} = 8.0 - 450V
R_{EN}	Pin PWMD pull-down resistance at PWMD	-	50	100	150	kΩ	V_{PWMD} = 5.0V
Current Sense Comparator							
$V_{CS,TH}$	Current sense pull-in threshold voltage	-	225	250	275	mV	-40°C < T_A < +85°C
			213	250	287		T_A < +125°C
V_{OFFSET}	Offset voltage for LD comparator	*	-12	-	12	mV	---
T_{BLANK}	Current sense blanking interval	-	150	215	280	ns	0 < T_A < +85°C, V_{LD} = V_{DD}, V_{CS} = $V_{CS,TH}$ + 50mV after T_{BLANK}
		-	145	215	315		-40 < T_A < +125°C, V_{LD} = V_{DD}, V_{CS} = $V_{CS,TH}$ + 50mV after T_{BLANK}
t_{DELAY}	Delay to output	-	-	80	150	ns	V_{LD} = V_{DD}, V_{CS} = $V_{CS,TH}$ + 50mV after T_{BLANK}
Oscillator							
f_{OSC}	Oscillator frequency	-	20	25	30	kHz	R_T = 1.00MΩ
		-	80	100	120		R_T = 226kΩ
GATE Driver							
I_{SOURCE}	GATE sourcing current	-	165	-	-	mA	V_{GATE} = 0V, V_{DD} = 7.5V
I_{SINK}	GATE sinking current	-	165	-	-	mA	V_{GATE} = V_{DD}, V_{DD} = 7.5V
t_{RISE}	GATE output rise time	-	-	30	50	ns	C_{GATE} = 500pF, V_{DD} = 7.5V
t_{FALL}	GATE output fall time	-	-	30	50	ns	C_{GATE} = 500pF, V_{DD} = 7.5V

Notes:

1. *Also limited by package power dissipation limit, whichever is lower.*

† *V_{DD} load current external to the HV9910B.*

* *Denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C.*

\# *Guaranteed by design.*

Application Information

The HV9910B is optimized to drive buck LED drivers using open-loop peak current mode control. This method of control enables fairly accurate LED current control without the need for high side current sensing or the design of any closed loop controllers. The IC uses very few external components and enables both Linear and PWM dimming of the LED current.

A resistor connected to the RT pin programs the frequency of operation (or the off-time). The oscillator produces pulses at regular intervals. These pulses set the SR flip-flop in the HV9910B which causes the GATE driver to turn on. The same pulses also start the blanking timer which inhibits the reset input of the SR flip flop and prevent false turn-offs due to the turn-on spike. When the FET turns on, the current through the inductor starts ramping up. This current flows through the external sense resistor R_{CS} and produces a ramp voltage at the CS pin. The comparators are constantly comparing the CS pin voltage to both the voltage at the LD pin and the internal 250mV. Once the blanking timer is complete, the output of these comparators is allowed to reset the flip flop. When the output of either one of the two comparators goes high, the flip flop is reset and the GATE output goes low. The GATE goes low until the SR flip flop is set by the oscillator. Assuming a 30% ripple in the inductor, the current sense resistor R_{CS} can be set using:

$$R_{CS} = \frac{0.25V \text{ (or } V_{LD})}{1.15 \bullet I_{LED} \text{ (A)}}$$

Constant frequency peak current mode control has an inherent disadvantage – at duty cycles greater than 0.5, the control scheme goes into subharmonic oscillations. To prevent this, an artificial slope is typically added to the current sense waveform. This slope compensation scheme will affect the accuracy of the LED current in the present form. However, a constant off-time peak current control scheme does not have this problem and can easily operate at duty cycles greater then 0.5 and also gives inherent input voltage rejection making the LED current almost insensitive to input voltage variations. But, it leads to variable frequency operation and the frequency range depends greatly on the input and output voltage variation. HV9910B makes it easy to switch between the two modes of operation by changing one connection (see oscillator section).

Input Voltage Regulator

The HV9910B can be powered directly from its VIN pin and can work from 8.0 - 450VDC at its VIN pin. When a voltage is applied at the VIN pin, the HV9910B maintains a constant 7.5V at the VDD pin. This voltage is used to power the IC and any external resistor dividers needed to control the IC. The VDD pin must be bypassed by a low ESR capacitor to provide a low impedance path for the high frequency current of the output GATE driver.

The HV9910B can also be operated by supplying a voltage at the VDD pin greater than the internally regulated voltage. This will turn off the internal linear regulator of the IC and the HV9910B will operate directly off the voltage supplied at the VDD pin. Please note that this external voltage at the VDD pin should not exceed 12V.

Although the VIN pin of the HV9910B is rated up to 450V, the actual maximum voltage that can be applied is limited by the power dissipation in the IC. For example, if an 8-pin SOIC (junction to ambient thermal resistance $R_{\theta,j\text{-}a}$ = 128°C/W) HV9910B draws about I_{IN} = 2.0mA from the VIN pin, and has a maximum allowable temperature rise of the junction temperature limited to about ΔT = 100°C, the maximum voltage at the VIN pin would be:

$$V_{IN(MAX)} = \frac{\Delta T}{R_{\theta,j-a}} \cdot \frac{1}{I_{in}}$$

$$= \frac{100°C}{128°C/W} \cdot \frac{1}{2mA}$$

$$= 390V.$$

In these cases, to operate the HV9910B from higher input voltages, a Zener diode can be added in series with the VIN pin to divert some of the power loss from the HV9910B to the Zener diode. In the above example, using a 100V zener diode will allow the circuit to easily work up to 450V.

The input current drawn from the VIN pin is a sum of the 1.0mA current drawn by the internal circuit and the current drawn by the GATE driver (which in turn depends on the switching frequency and the GATE charge of the external FET).

$$I_{IN} \approx 1.0mA + Q_G \bullet f_S$$

In the above equation, f_S is the switching frequency and Q_G is the GATE charge of the external FET (which can be obtained from the datasheet of the FET).

Current Sense

The current sense input of the HV9910B goes to the non-inverting inputs of two comparators. The inverting terminal of one comparator is tied to an internal 250mV reference whereas the inverting terminal of the other comparator is connected to the LD pin. The outputs of both these comparators are fed into an OR GATE and the output of the OR GATE is fed into the reset pin of the flip-flop. Thus, the comparator which has the lowest voltage at the inverting terminal determines when the GATE output is turned off.

The outputs of the comparators also include a 150-280ns blanking time which prevents spurious turn-offs of the external FET due to the turn-on spike normally present in peak current mode control. In rare cases, this internal blanking might not be enough to filter out the turn-on spike. In these cases, an external RC filter needs to be added between the external sense resistor (R_{CS}) and the CS pin.

Please note that the comparators are fast (with a typical 80ns response time). Hence these comparators are more susceptible to be triggered by noise than the comparators of the HV9910. A proper layout minimizing external inductances will prevent false triggering of these comparators.

Oscillator

The oscillator in the HV9910B is controlled by a single resistor connected at the RT pin. The equation governing the oscillator time period t_{OSC} is given by:

$$t_{OSC}(\mu s) = \frac{R_T(k\Omega) + 22}{25}$$

If the resistor is connected between RT and GND, HV9910B operates in a constant frequency mode and the above equation determines the time-period. If the resistor is connected between RT and GATE, the HV9910B operates in a constant off-time mode and the above equation determines the off-time.

GATE Output

The GATE output of the HV9910B is used to drive an external FET. It is recommended that the GATE charge of the external FET be less than 25nC for switching frequencies ≤100kHz and less than 15nC for switching frequencies > 100kHz.

Linear Dimming

The Linear Dimming pin is used to control the LED current. There are two cases when it may be necessary to use the Linear Dimming pin.

- In some cases, it may not be possible to find the exact R_{CS} value required to obtain the LED current when the internal 250mV is used. In these cases, an external voltage divider from the VDD pin can be connected to the LD pin to obtain a voltage (less than 250mV) corresponding to the desired voltage across R_{CS}.

- Linear dimming may be desired to adjust the current level to reduce the intensity of the LEDs. In these cases, an external 0-250mV voltage can be connected to the LD pin to adjust the LED current during operation.

To use the internal 250mV, the LD pin can be connected to VDD.

Note:

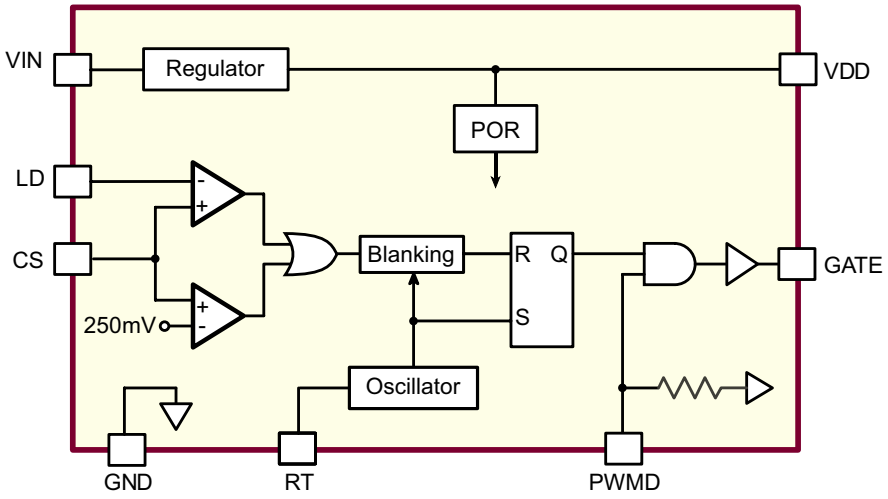
Although the LD pin can be pulled to GND, the output current will not go to zero. This is due to the presence of a minimum on-time (which is equal to the sum of the blanking time and the delay to output time) which is about 450ns. This will cause the FET to be on for a minimum of 450ns and thus the LED current when LD = GND will not be zero. This current is also dependent on the input voltage, inductance value, forward voltage of the LEDs and circuit parasitics. To get zero LED current, the PWMD pin has to be used.

PWM Dimming

PWM Dimming can be achieved by driving the PWMD pin with a low frequency square wave signal. When the PWM signal is zero, the GATE driver is turned off and when the PWMD signal if high, the GATE driver is enabled. Since the PWMD signal does not turn off the other parts of the IC, the response of the HV9910B to the PWMD signal is almost instantaneous. The rate of rise and fall of the LED current is thus determined solely by the rise and fall times of the inductor current.

To disable PWM dimming and enable the HV9910B permanently, connect the PWMD pin to VDD.

Block Diagram

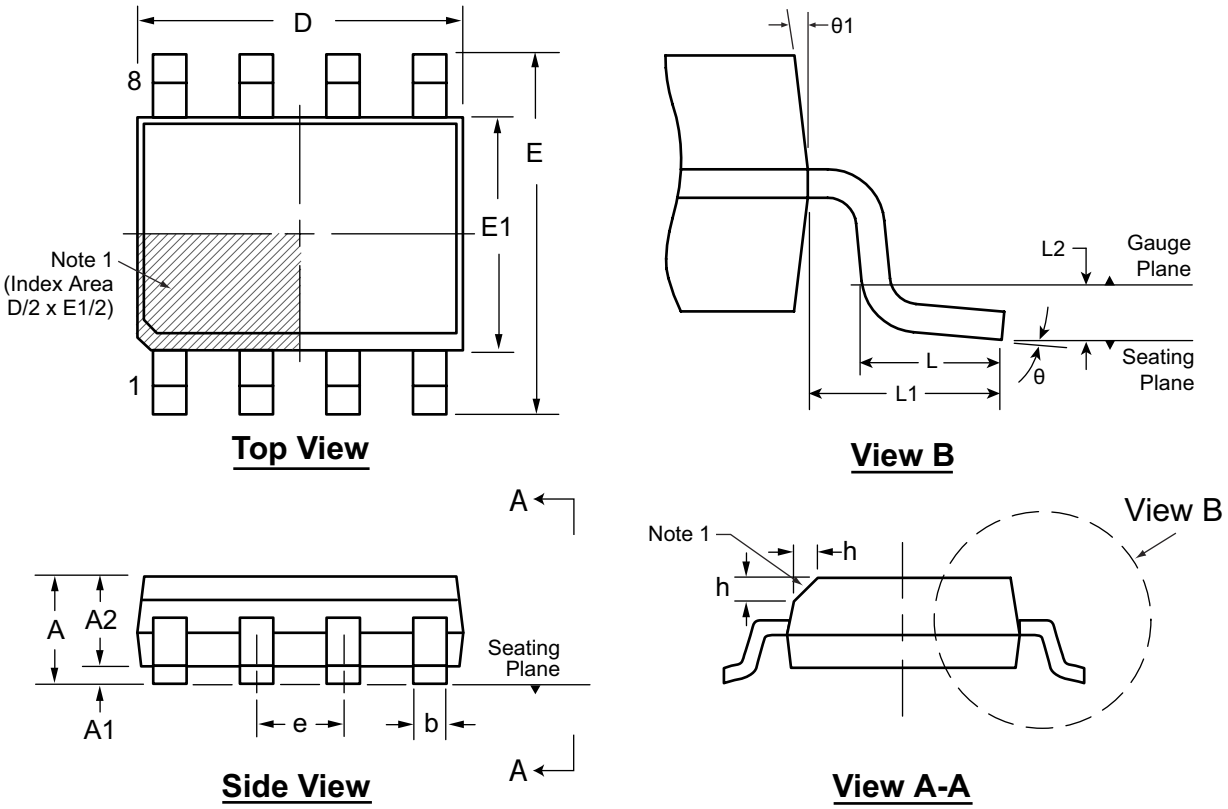


Pin Description

Pin #		Function	Description
8-Lead SOIC	16-Lead SOIC		
1	1	VIN	This pin is the input of an 8.0 - 450V linear regulator.
2	4	CS	This pin is the current sense pin used to sense the FET current by means of an external sense resistor. When this pin exceeds the lower of either the internal 250mV or the voltage at the LD pin, the GATE output goes low.
3	5	GND	Ground return for all internal circuitry. This pin must be electrically connected to the ground of the power train.
4	8	GATE	This pin is the output GATE driver for an external N-channel power MOSFET.
5	9	PWMD	This is the PWM dimming input of the IC. When this pin is pulled to GND, the GATE driver is turned off. When the pin is pulled high, the GATE driver operates normally.
6	12	VDD	This is the power supply pin for all internal circuits. It must be bypassed with a low ESR capacitor to GND (≥0.1µF).
7	13	LD	This pin is the linear dimming input and sets the current sense threshold as long as the voltage at the pin is less than 250mV (typ).
8	14	RT	This pin sets the oscillator frequency. When a resistor is connected between RT and GND, the HV9910B operates in constant frequency mode. When the resistor is connected between RT and GATE, the IC operates in constant off-time mode.
-	2, 3, 6, 7, 10, 11, 15, 16	NC	No connection

8-Lead SOIC (Narrow Body) Package Outline (LG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note:

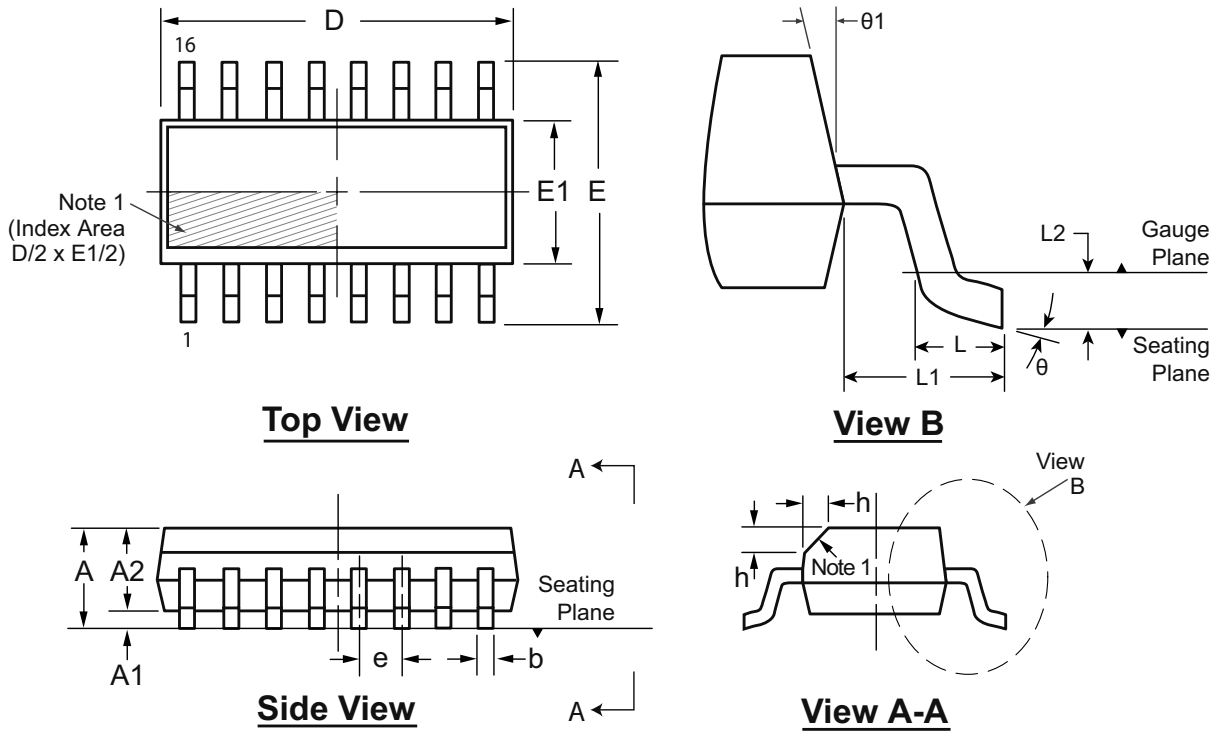
1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
Supertex Doc. #: *DSPD-8SOLGTG, Version I041309.*

16-Lead SOIC (Narrow Body) Package Outline (NG)

9.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note:

1. *This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	9.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	9.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	10.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AC, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
***Supertex Doc. #:** DSPD-16SONG, Version G041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
www.supertex.com