

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## HEF4526B

### MSI

## Programmable 4-bit binary down counter

Product specification  
File under Integrated Circuits, IC04

January 1995

## Programmable 4-bit binary down counter

**HEF4526B**  
**MSI**

### DESCRIPTION

The HEF4526B is a synchronous programmable 4-bit binary down counter with an active HIGH and an active LOW clock input ( $CP_0$ ,  $\overline{CP}_1$ ), an asynchronous parallel load input (PL), four parallel inputs ( $P_0$  to  $P_3$ ), a cascade feedback input (CF), four buffered parallel outputs ( $O_0$  to  $O_3$ ), a terminal count output (TC) and an overriding asynchronous master reset input (MR).

This device is a programmable, cascadable down counter with a decoded TC output for divide-by-n applications. In single stage applications the TC output is connected to PL. CF allows cascade divide-by-n operation with no additional gates required.

Information on  $P_0$  to  $P_3$  is loaded into the counter while PL is HIGH, independent of all other input conditions except MR, which must be LOW. When PL and  $\overline{CP}_1$  are LOW, the counter advances on a LOW to HIGH transition of  $CP_0$ . When PL is LOW and  $CP_0$  is HIGH, the counter advances on a HIGH to LOW transition of  $\overline{CP}_1$ . TC is HIGH when the counter is in the zero state ( $O_0 = O_1 = O_2 = O_3 = \text{LOW}$ ) and CF is HIGH and PL is LOW. A HIGH on MR resets the counter ( $O_0$  to  $O_3 = \text{LOW}$ ) independent of other input conditions.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

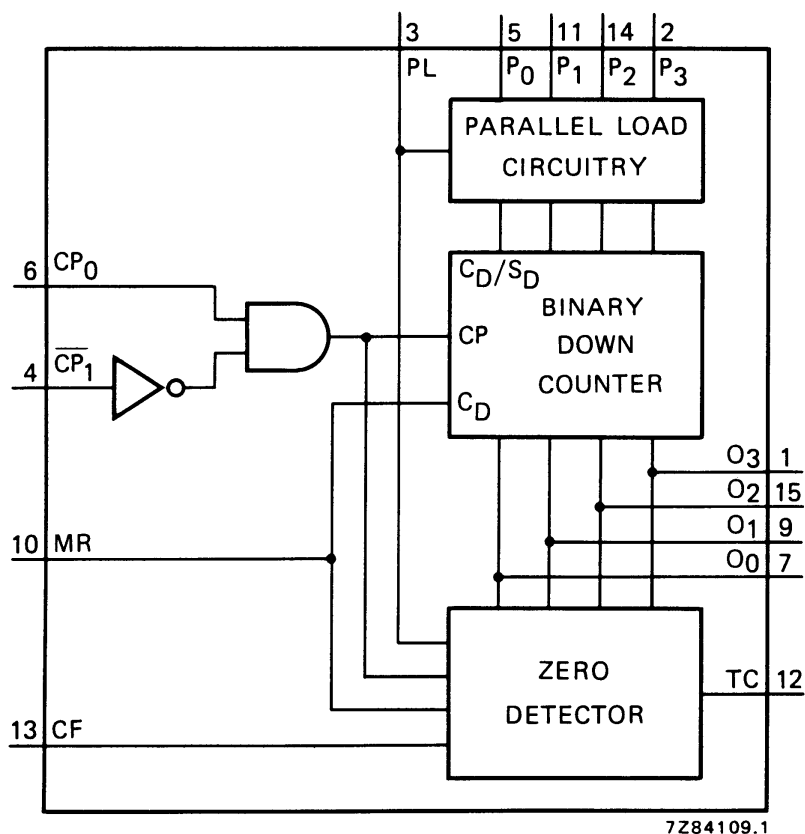


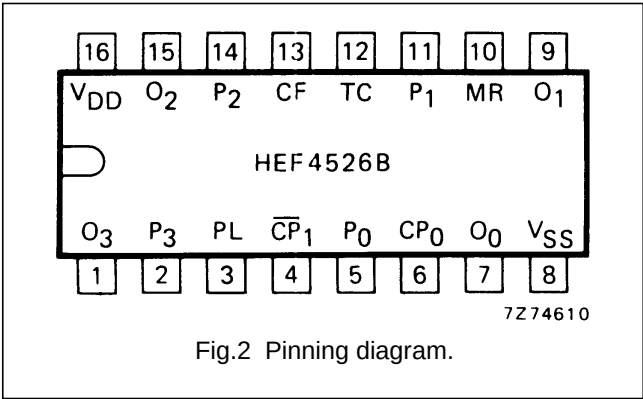
Fig.1 Functional diagram.

### FAMILY DATA, $I_{DD}$ LIMITS category MSI

See Family Specifications

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MSI



HEF4526BP(N): 16-lead DIL; plastic (SOT38-1)  
HEF4526BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)  
HEF4526BT(D): 16-lead SO; plastic (SOT109-1)  
( ): Package Designator North America

PINNING

- PL parallel load input
- P<sub>0</sub> to P<sub>3</sub> parallel inputs
- CF cascade feedback input
- CP<sub>0</sub> clock input (LOW to HIGH, triggered)
- CP<sub>1</sub> clock input (HIGH to LOW, triggered)
- MR asynchronous master reset input
- TC terminal count output
- O<sub>0</sub> to O<sub>3</sub> buffered parallel outputs

COUNTING MODE

CF = HIGH; PL = LOW; MR = LOW

| COUNT | OUTPUTS        |                |                |                |
|-------|----------------|----------------|----------------|----------------|
|       | O <sub>3</sub> | O <sub>2</sub> | O <sub>1</sub> | O <sub>0</sub> |
| 15    | H              | H              | H              | H              |
| 14    | H              | H              | H              | L              |
| 13    | H              | H              | L              | H              |
| 12    | H              | H              | L              | L              |
| 11    | H              | L              | H              | H              |
| 10    | H              | L              | H              | L              |
| 9     | H              | L              | L              | H              |
| 8     | H              | L              | L              | L              |
| 7     | L              | H              | H              | H              |
| 6     | L              | H              | H              | L              |
| 5     | L              | H              | L              | H              |
| 4     | L              | H              | L              | L              |
| 3     | L              | L              | H              | H              |
| 2     | L              | L              | H              | L              |
| 1     | L              | L              | L              | H              |
| 0     | L              | L              | L              | L              |

FUNCTION TABLE

| MR | PL | CP <sub>0</sub> | CP <sub>1</sub> | MODE                  |
|----|----|-----------------|-----------------|-----------------------|
| H  | X  | X               | X               | reset (asynchronous)  |
| L  | H  | X               | X               | preset (asynchronous) |
| L  | L  | ↗               | H               | no change             |
| L  | L  | L               | ↘               | no change             |
| L  | L  | ↘               | X               | no change             |
| L  | L  | X               | ↗               | no change             |
| L  | L  | ↗               | L               | counter advances      |
| L  | L  | H               | ↘               | counter advances      |

Notes

- 1. H = HIGH state (the more positive voltage)  
L = LOW state (the less positive voltage)  
X = state is immaterial  
↗ = positive-going transition  
↘ = negative-going transition

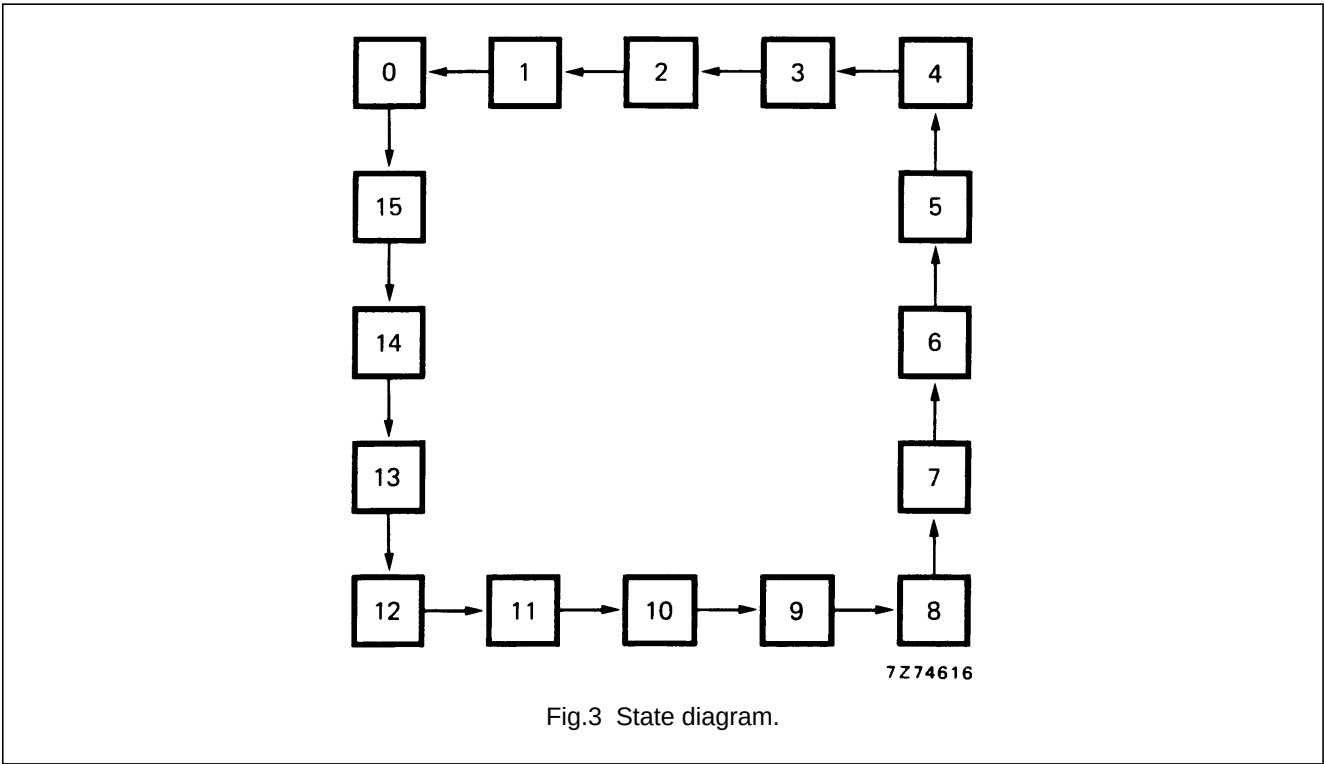
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SINGLE STAGE OPERATION

Divide-by-n; MR = LOW; CF = HIGH;  $\overline{CP_1}$  = LOW

| PL | P <sub>3</sub> | P <sub>2</sub> | P <sub>1</sub> | P <sub>0</sub> | DIVIDE BY    | TC OUTPUT PULSE WIDTH |
|----|----------------|----------------|----------------|----------------|--------------|-----------------------|
| L  | X              | X              | X              | X              | 16           | one clock period      |
| TC | H              | H              | H              | H              | 15           | clock pulse HIGH      |
| TC | H              | H              | H              | L              | 14           |                       |
| TC | H              | H              | L              | H              | 13           |                       |
| TC | H              | H              | L              | L              | 12           |                       |
| TC | H              | L              | H              | H              | 11           |                       |
| TC | H              | L              | H              | L              | 10           |                       |
| TC | H              | L              | L              | H              | 9            |                       |
| TC | H              | L              | L              | L              | 8            |                       |
| TC | L              | H              | H              | H              | 7            |                       |
| TC | L              | H              | H              | L              | 6            |                       |
| TC | L              | H              | L              | H              | 5            |                       |
| TC | L              | H              | L              | L              | 4            |                       |
| TC | L              | L              | H              | H              | 3            |                       |
| TC | L              | L              | H              | L              | 2            |                       |
| TC | L              | L              | L              | H              | 1            |                       |
| TC | L              | L              | L              | L              | no operation |                       |



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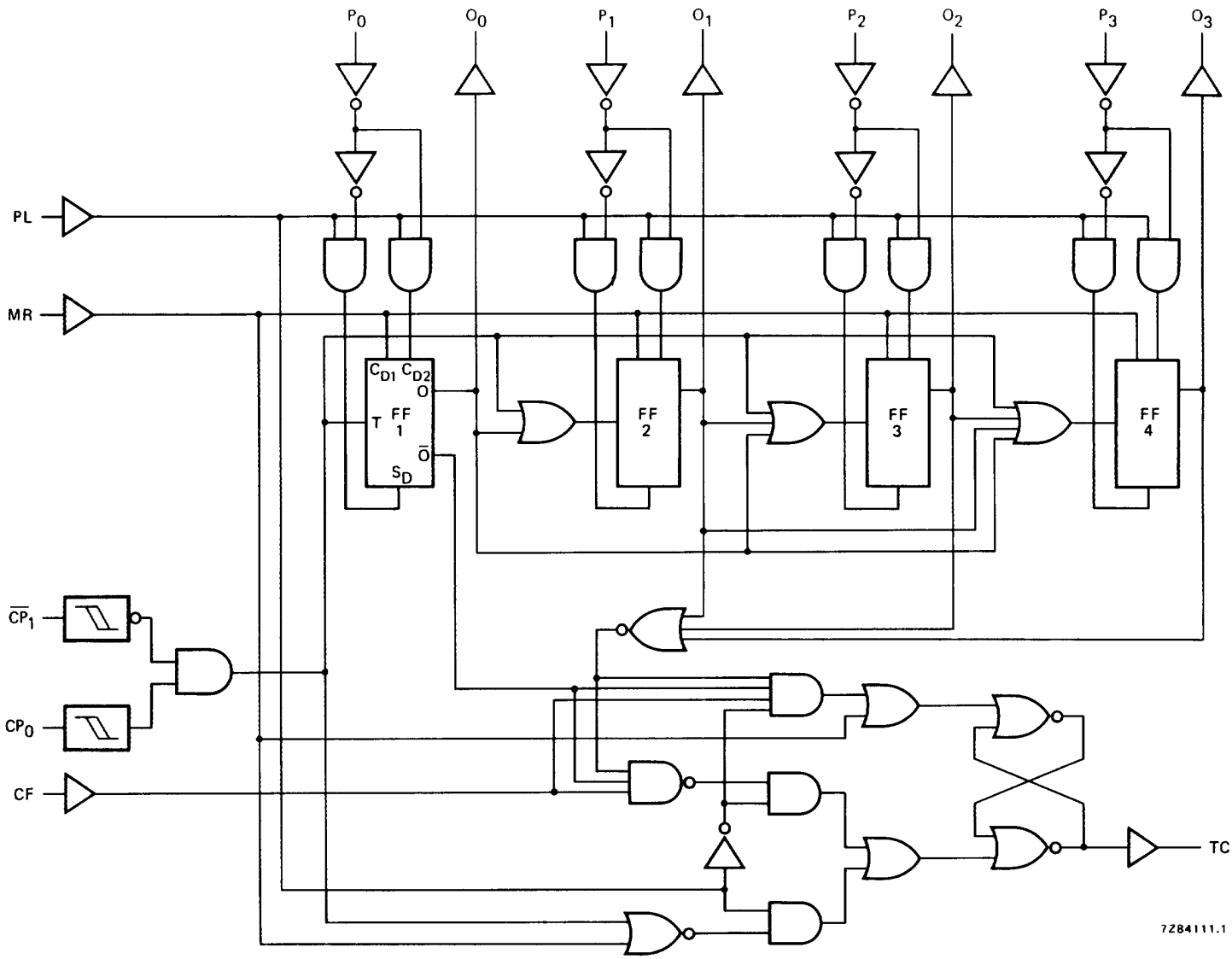


Fig.4 Logic diagram.

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## AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; input transition times  $\leq 20\text{ ns}$ 

|                                                 | $V_{DD}$<br>V | TYPICAL FORMULA FOR P ( $\mu\text{W}$ )                                                                                                      |                                                                                                                                                                         |
|-------------------------------------------------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Dynamic power<br>dissipation per<br>package (P) | 5<br>10<br>15 | $1000 f_i + \sum (f_o C_L) \times V_{DD}^2$<br>$4000 f_i + \sum (f_o C_L) \times V_{DD}^2$<br>$10\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$ | where<br>$f_i$ = input freq. (MHz)<br>$f_o$ = output freq. (MHz)<br>$C_L$ = load capacitance (pF)<br>$\sum (f_o C_L)$ = sum of outputs<br>$V_{DD}$ = supply voltage (V) |

## AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$ 

|                                                     | V <sub>DD</sub><br>V | SYMBOL           | MIN. | TYP. | MAX. | TYPICAL EXTRAPOLATION<br>FORMULA |                                      |
|-----------------------------------------------------|----------------------|------------------|------|------|------|----------------------------------|--------------------------------------|
| Propagation delays                                  |                      |                  |      |      |      |                                  |                                      |
| CP <sub>0</sub> , $\overline{CP_1} \rightarrow O_n$ | 5                    |                  |      | 150  | 300  | ns                               | 123 ns + (0,55 ns/pF) C <sub>L</sub> |
| HIGH to LOW                                         | 10                   | t <sub>PHL</sub> |      | 65   | 130  | ns                               | 54 ns + (0,23 ns/pF) C <sub>L</sub>  |
|                                                     | 15                   |                  |      | 50   | 100  | ns                               | 42 ns + (0,16 ns/pF) C <sub>L</sub>  |
| LOW to HIGH                                         | 5                    |                  |      | 150  | 300  | ns                               | 123 ns + (0,55 ns/pF) C <sub>L</sub> |
|                                                     | 10                   | t <sub>PLH</sub> |      | 65   | 130  | ns                               | 54 ns + (0,23 ns/pF) C <sub>L</sub>  |
|                                                     | 15                   |                  |      | 50   | 100  | ns                               | 42 ns + (0,16 ns/pF) C <sub>L</sub>  |
| CP <sub>0</sub> , $\overline{CP_1} \rightarrow TC$  | 5                    |                  |      | 210  | 420  | ns                               | 183 ns + (0,55 ns/pF) C <sub>L</sub> |
| HIGH to LOW                                         | 10                   | t <sub>PHL</sub> |      | 90   | 180  | ns                               | 79 ns + (0,23 ns/pF) C <sub>L</sub>  |
|                                                     | 15                   |                  |      | 70   | 140  | ns                               | 62 ns + (0,16 ns/pF) C <sub>L</sub>  |
| LOW to HIGH                                         | 5                    |                  |      | 210  | 420  | ns                               | 183 ns + (0,55 ns/pF) C <sub>L</sub> |
|                                                     | 10                   | t <sub>PLH</sub> |      | 90   | 180  | ns                               | 79 ns + (0,23 ns/pF) C <sub>L</sub>  |
|                                                     | 15                   |                  |      | 70   | 140  | ns                               | 62 ns + (0,16 ns/pF) C <sub>L</sub>  |
| PL → O <sub>n</sub>                                 | 5                    |                  |      | 200  | 400  | ns                               | 173 ns + (0,55 ns/pF) C <sub>L</sub> |
| HIGH to LOW                                         | 10                   | t <sub>PHL</sub> |      | 80   | 160  | ns                               | 69 ns + (0,23 ns/pF) C <sub>L</sub>  |
|                                                     | 15                   |                  |      | 60   | 120  | ns                               | 52 ns + (0,16 ns/pF) C <sub>L</sub>  |
| LOW to HIGH                                         | 5                    |                  |      | 180  | 360  | ns                               | 153 ns + (0,55 ns/pF) C <sub>L</sub> |
|                                                     | 10                   | t <sub>PLH</sub> |      | 70   | 140  | ns                               | 59 ns + (0,23 ns/pF) C <sub>L</sub>  |
|                                                     | 15                   |                  |      | 50   | 100  | ns                               | 42 ns + (0,16 ns/pF) C <sub>L</sub>  |
| MR → O <sub>n</sub>                                 | 5                    |                  |      | 140  | 280  | ns                               | 113 ns + (0,55 ns/pF) C <sub>L</sub> |
| HIGH to LOW                                         | 10                   | t <sub>PHL</sub> |      | 55   | 110  | ns                               | 44 ns + (0,23 ns/pF) C <sub>L</sub>  |
|                                                     | 15                   |                  |      | 40   | 80   | ns                               | 32 ns + (0,16 ns/pF) C <sub>L</sub>  |
| Output transition times                             | 5                    |                  |      | 60   | 120  | ns                               | 10 ns + (1,0 ns/pF) C <sub>L</sub>   |
| HIGH to LOW                                         | 10                   | t <sub>THL</sub> |      | 30   | 60   | ns                               | 9 ns + (0,42 ns/pF) C <sub>L</sub>   |
|                                                     | 15                   |                  |      | 20   | 40   | ns                               | 6 ns + (0,28 ns/pF) C <sub>L</sub>   |
| LOW to HIGH                                         | 5                    |                  |      | 60   | 120  | ns                               | 10 ns + (1,0 ns/pF) C <sub>L</sub>   |
|                                                     | 10                   | t <sub>TLH</sub> |      | 30   | 60   | ns                               | 9 ns + (0,42 ns/pF) C <sub>L</sub>   |
|                                                     | 15                   |                  |      | 20   | 40   | ns                               | 6 ns + (0,28 ns/pF) C <sub>L</sub>   |

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## AC CHARACTERISTICS

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$

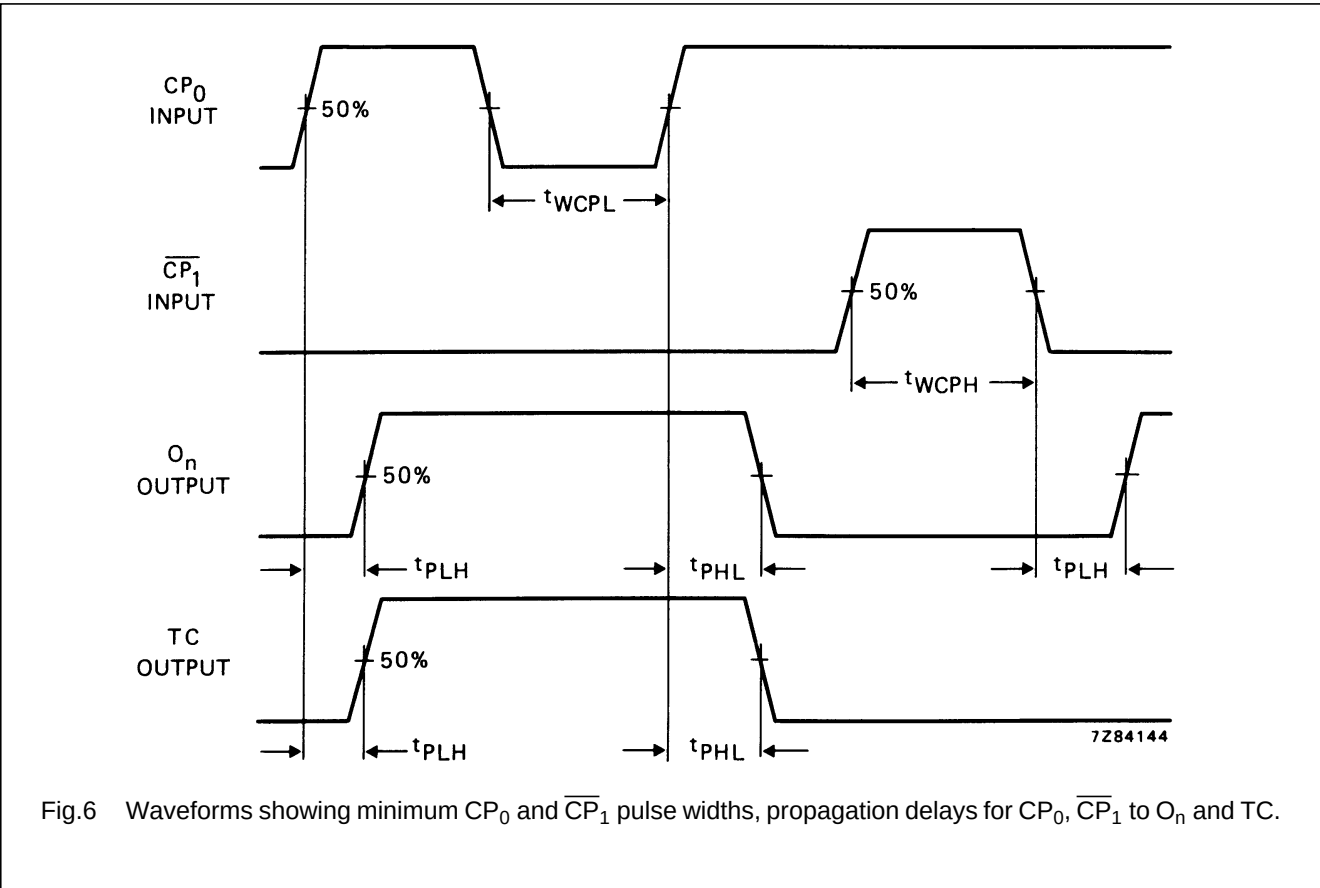
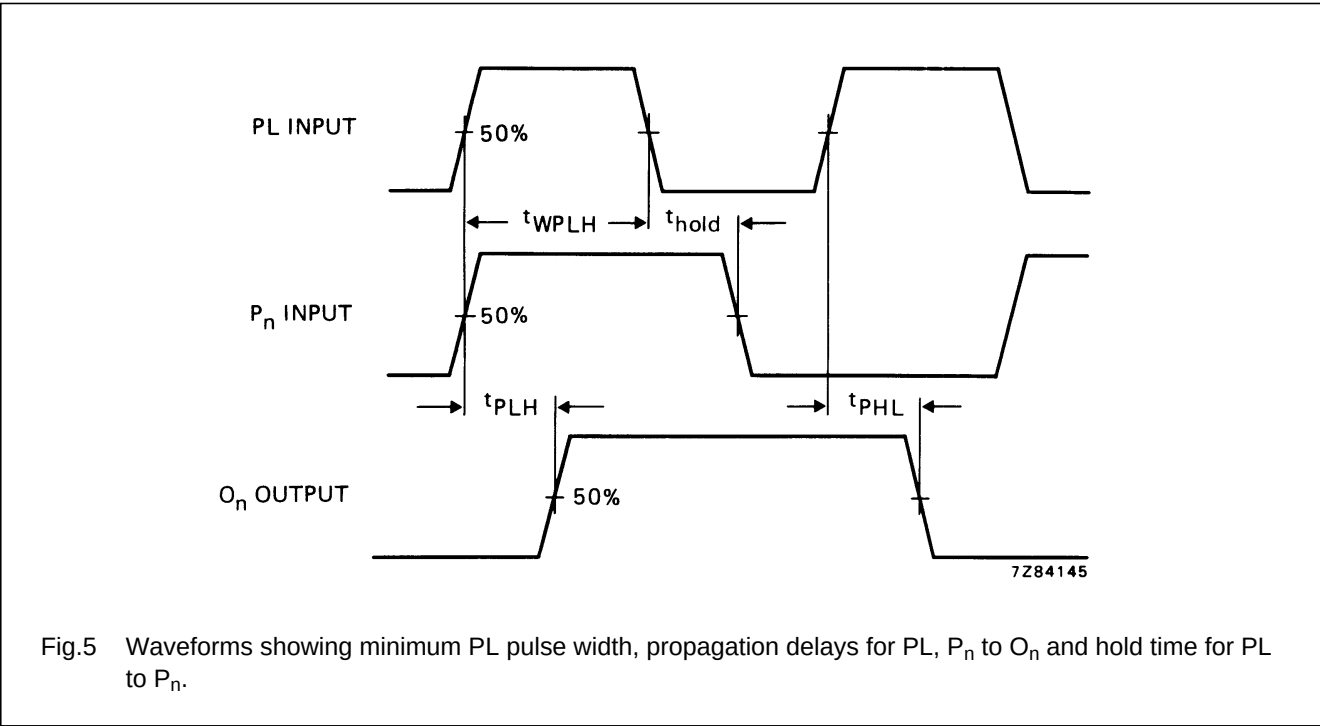
|                                                        | $V_{DD}$<br>V | SYMBOL     | MIN. | TYP. | MAX. |                                    |
|--------------------------------------------------------|---------------|------------|------|------|------|------------------------------------|
| Minimum clock<br>pulse width $CP_0$<br>LOW             | 5             | $t_{WCPL}$ | 80   | 40   | ns   | see also waveforms<br>Figs 5 and 6 |
|                                                        | 10            |            | 40   | 20   | ns   |                                    |
|                                                        | 15            |            | 30   | 15   | ns   |                                    |
| Minimum clock<br>pulse width $\overline{CP}_1$<br>HIGH | 5             | $t_{WCPH}$ | 80   | 40   | ns   |                                    |
|                                                        | 10            |            | 40   | 20   | ns   |                                    |
|                                                        | 15            |            | 30   | 15   | ns   |                                    |
| Minimum PL<br>pulse width; HIGH                        | 5             | $t_{WPLH}$ | 100  | 50   | ns   |                                    |
|                                                        | 10            |            | 40   | 20   | ns   |                                    |
|                                                        | 15            |            | 32   | 16   | ns   |                                    |
| Minimum MR<br>pulse width; HIGH                        | 5             | $t_{WMRH}$ | 130  | 65   | ns   |                                    |
|                                                        | 10            |            | 50   | 25   | ns   |                                    |
|                                                        | 15            |            | 40   | 20   | ns   |                                    |
| Hold time<br>$P_n \rightarrow PL$                      | 5             | $t_{hold}$ | 30   | 5    | ns   |                                    |
|                                                        | 10            |            | 20   | 5    | ns   |                                    |
|                                                        | 15            |            | 15   | 5    | ns   |                                    |
| Set-up time<br>$P_n \rightarrow PL$                    | 5             | $t_{su}$   | 30   | 0    | ns   |                                    |
|                                                        | 10            |            | 20   | 0    | ns   |                                    |
|                                                        | 15            |            | 15   | 0    | ns   |                                    |
| Maximum clock<br>pulse frequency<br>PL = LOW           | 5             | $f_{max}$  | 6    | 12   | MHz  | see note 1                         |
|                                                        | 10            |            | 12   | 25   | MHz  |                                    |
|                                                        | 15            |            | 16   | 32   | MHz  |                                    |

## Note

1. In the divide-by-n mode (PL connected to TC), one has to observe the maximum HIGH to LOW propagation delay for CP to TC, before applying the next clock pulse.

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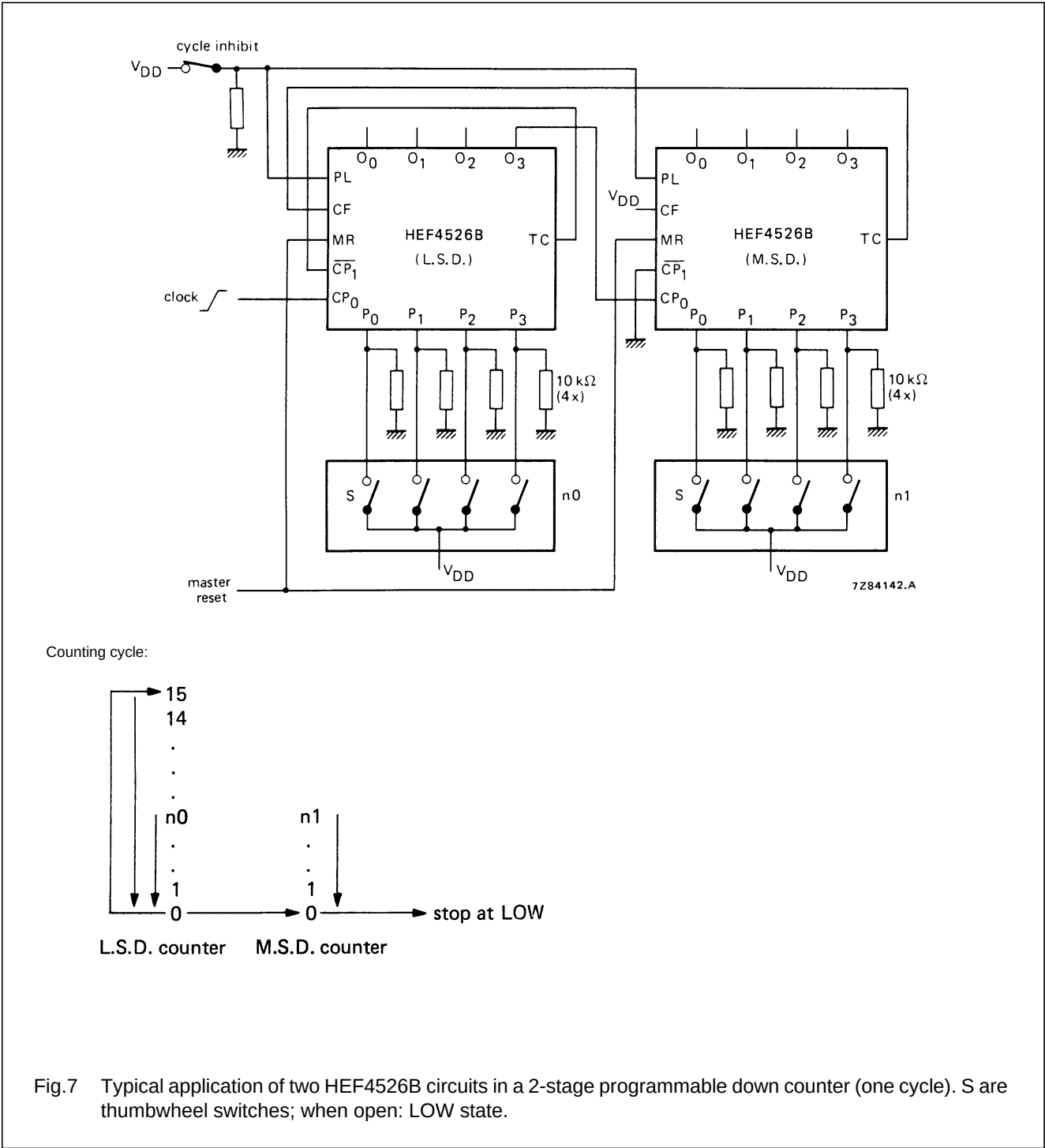
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APPLICATION INFORMATION

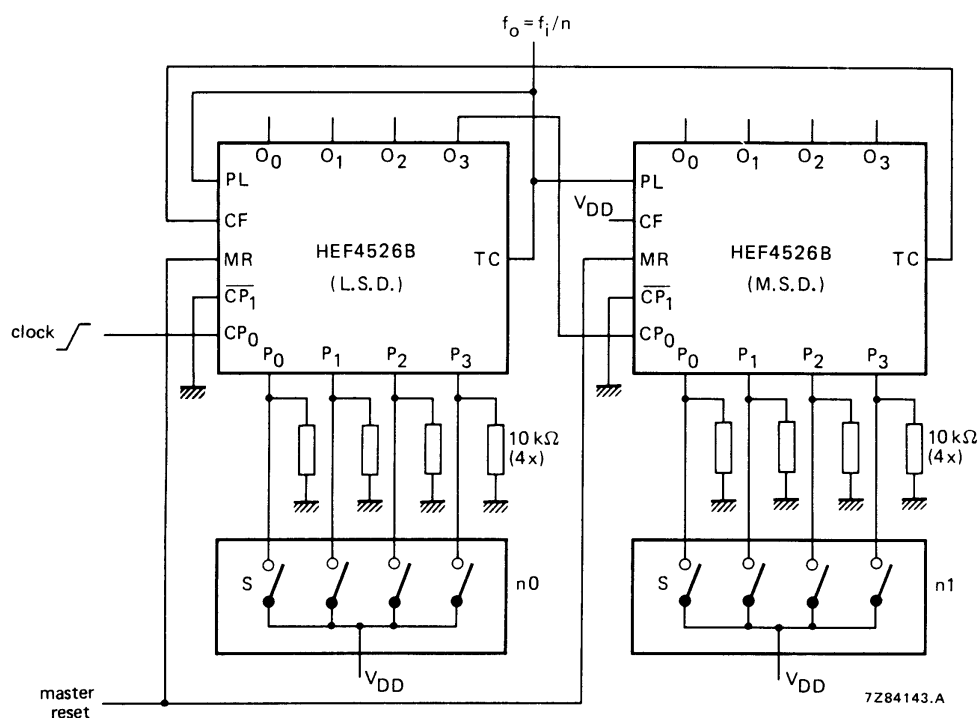
Some examples of applications for the HEF4526B are:

- Divide-by-n counter
- Programmable frequency divider



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Counting cycle:

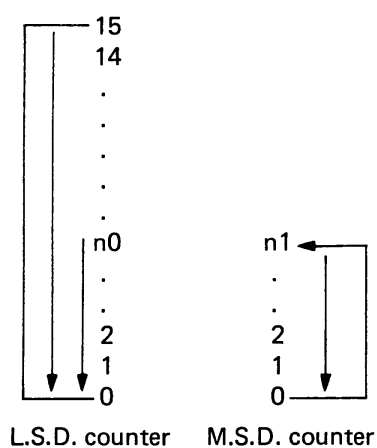


Fig.8 Typical application of two HEF4526B circuits in a 2-stage programmable frequency divider. S are thumbwheel switches; when open: LOW state.

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