DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4070B gates

Quadruple exclusive-OR gate

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

QUADRUPLE EXCLUSIVE-OR GATE

The HEF4070B provides the positive quadruple exclusive-OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

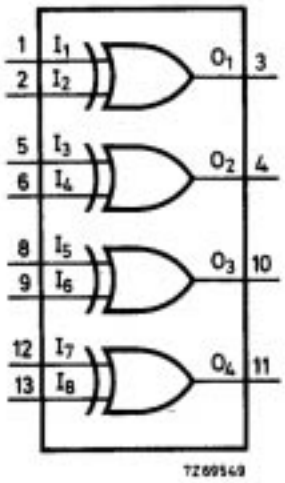

Fig. 1 Functional diagram.

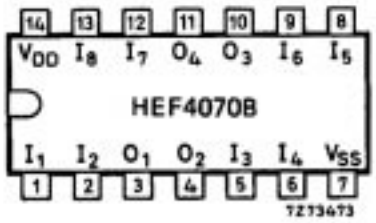

Fig. 2 Pinning diagram.

HEF4070BP(N): 14-lead DIL; plastic (SOT27-1)
HEF4070BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
HEF4070BT(D): 14-lead SO; plastic (SOT108-1)
( ): Package Designator North America

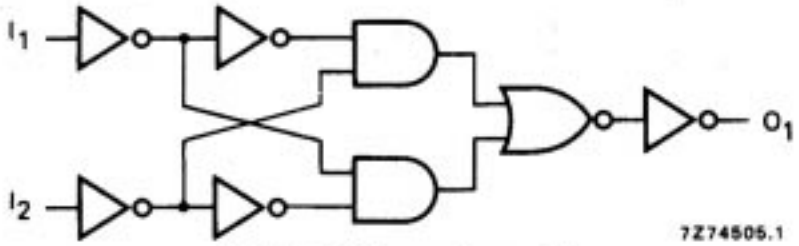

Fig. 3 Logic diagram (one gate).

APPLICATION INFORMATION

Some examples of applications for the HEF4070B are:

- Logical comparators
- Parity checkers and generators

TRUTH TABLE

I_1	I_2	O_1
L	L	L
H	L	H
L	H	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		85	175	ns	58 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	75	ns	24 ns + (0,23 ns/pF) C_L
	15		30	55	ns	21 ns + (0,16 ns/pF) C_L
	5		75	150	ns	48 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	65	ns	19 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$14\,400\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	