

# DATA SHEET

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- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## HEF4051B

### MSI

8-channel analogue  
multiplexer/demultiplexer

Product specification  
File under Integrated Circuits, IC04

January 1995

8-channel analogue multiplexer/demultiplexer

HEF4051B  
MSI

DESCRIPTION

The HEF4051B is an 8-channel analogue multiplexer/demultiplexer with three address inputs ( $A_0$  to  $A_2$ ), an active LOW enable input ( $\bar{E}$ ), eight independent inputs/outputs ( $Y_0$  to  $Y_7$ ) and a common input/output ( $Z$ ).

The device contains eight bidirectional analogue switches, each with one side connected to an independent input/output ( $Y_0$  to  $Y_7$ )

and the other side connected to a common input/output ( $Z$ ).

With  $\bar{E}$  LOW, one of the eight switches is selected (low impedance ON-state) by  $A_0$  to  $A_2$ . With  $\bar{E}$  HIGH, all switches are in the high impedance OFF-state, independent of  $A_0$  to  $A_2$ .

$V_{DD}$  and  $V_{SS}$  are the supply voltage connections for the digital control inputs ( $A_0$  to  $A_2$ , and  $\bar{E}$ ). The  $V_{DD}$  to  $V_{SS}$  range is 3 to 15 V.

The analogue inputs/outputs ( $Y_0$  to  $Y_7$ , and  $Z$ ) can swing between  $V_{DD}$  as a positive limit and  $V_{EE}$  as a negative limit.  $V_{DD}-V_{EE}$  may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer,  $V_{EE}$  is connected to  $V_{SS}$  (typically ground).

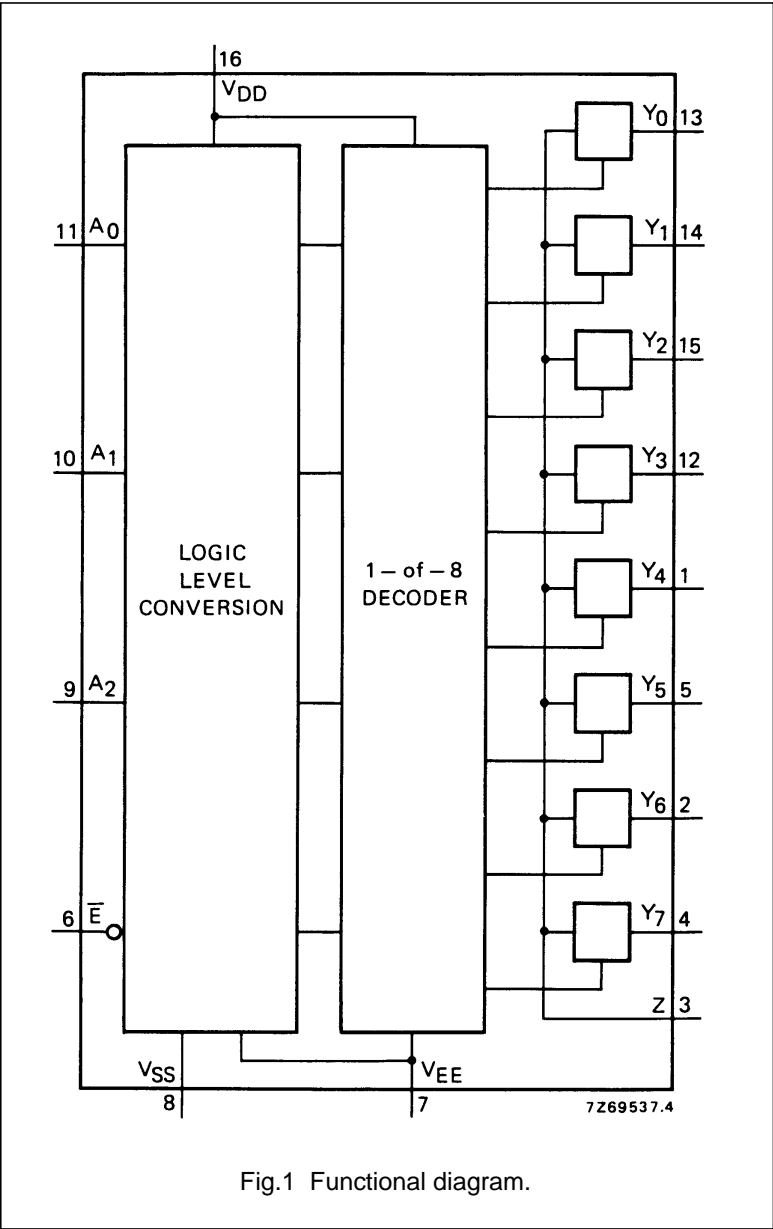


Fig.1 Functional diagram.

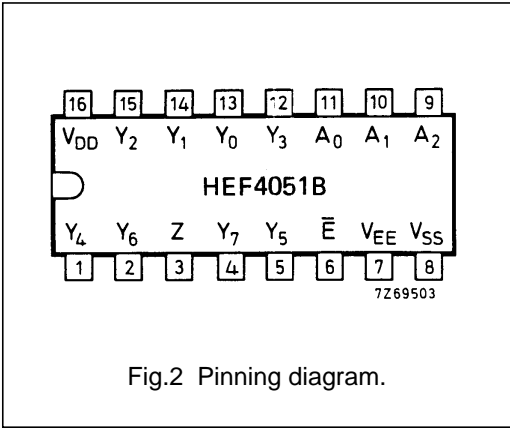


Fig.2 Pinning diagram.

- HEF4051BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4051BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4051BT(D): 16-lead SO; plastic (SOT109-1)
- ( ): Package Designator North America

PINNING

- $Y_0$  to  $Y_7$  independent inputs/outputs
- $A_0$  to  $A_2$  address inputs
- $\bar{E}$  enable input (active LOW)
- $Z$  common input/output

FAMILY DATA,  $I_{DD}$  LIMITS category MSI

See Family Specifications.

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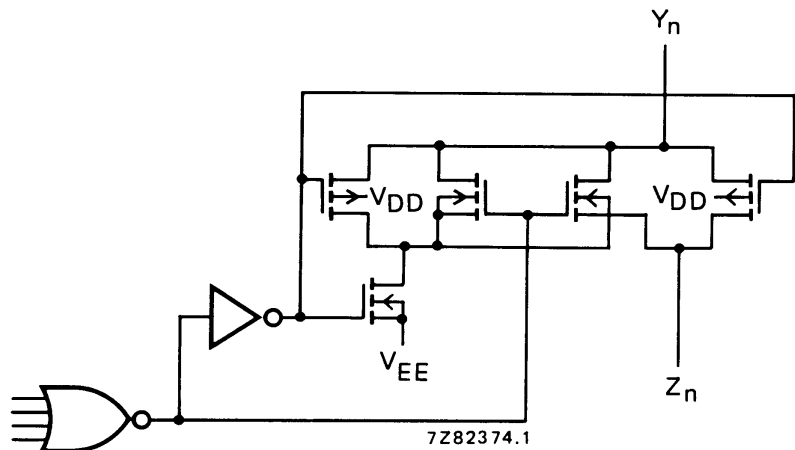


Fig.3 Schematic diagram (one switch).

FUNCTION TABLE

INPUTS				CHANNEL ON
$\bar{E}$	$A_2$	$A_1$	$A_0$	
L	L	L	L	$Y_0-Z$
L	L	L	H	$Y_1-Z$
L	L	H	L	$Y_2-Z$
L	L	H	H	$Y_3-Z$
L	H	L	L	$Y_4-Z$
L	H	L	H	$Y_5-Z$
L	H	H	L	$Y_6-Z$
L	H	H	H	$Y_7-Z$
H	X	X	X	none

Notes

- 1. H = HIGH state (the more positive voltage)  
L = LOW state (the less positive voltage)  
X = state is immaterial

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (with reference to  $V_{DD}$ )  $V_{EE}$  -18 to + 0,5 V

Note

- 1. To avoid drawing  $V_{DD}$  current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no  $V_{DD}$  current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed  $V_{DD}$  or  $V_{EE}$ .

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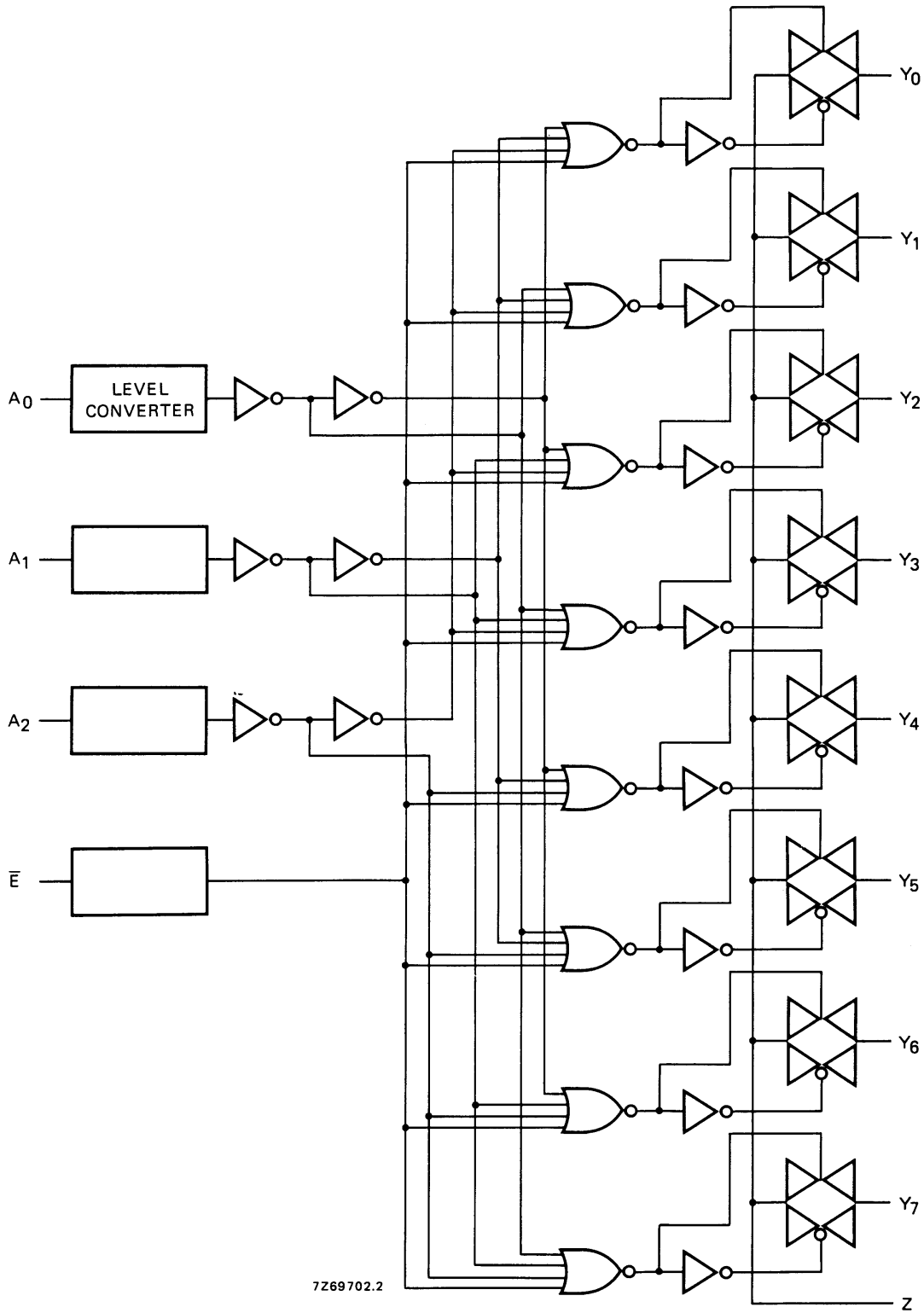


Fig.4 Logic diagram.

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DC CHARACTERISTICS

T<sub>amb</sub> = 25 °C

	$V_{DD}-V_{EE}$ V	SYMBOL	TYP.	MAX.		CONDITIONS
ON resistance	5	$R_{ON}$	350	2500	$\Omega$	$V_{is} = 0$ to $V_{DD}-V_{EE}$ see Fig.6
	10		80	245	$\Omega$	
	15		60	175	$\Omega$	
ON resistance	5	$R_{ON}$	115	340	$\Omega$	$V_{is} = 0$ see Fig.6
	10		50	160	$\Omega$	
	15		40	115	$\Omega$	
ON resistance	5	$R_{ON}$	120	365	$\Omega$	$V_{is} = V_{DD}-V_{EE}$ see Fig.6
	10		65	200	$\Omega$	
	15		50	155	$\Omega$	
'Δ' ON resistance between any two channels	5	$\Delta R_{ON}$	25	–	$\Omega$	$V_{is} = 0$ to $V_{DD}-V_{EE}$ see Fig.6
	10		10	–	$\Omega$	
	15		5	–	$\Omega$	
OFF-state leakage current, all channels OFF	5	$I_{OZZ}$	–	–	nA	$\bar{E}$ at $V_{DD}$ $V_{SS} = V_{EE}$
	10		–	–	nA	
	15		–	1000	nA	
OFF-state leakage current, any channel	5	$I_{OZY}$	–	–	nA	$\bar{E}$ at $V_{SS}$ $V_{SS} = V_{EE}$
	10		–	–	nA	
	15		–	200	nA	

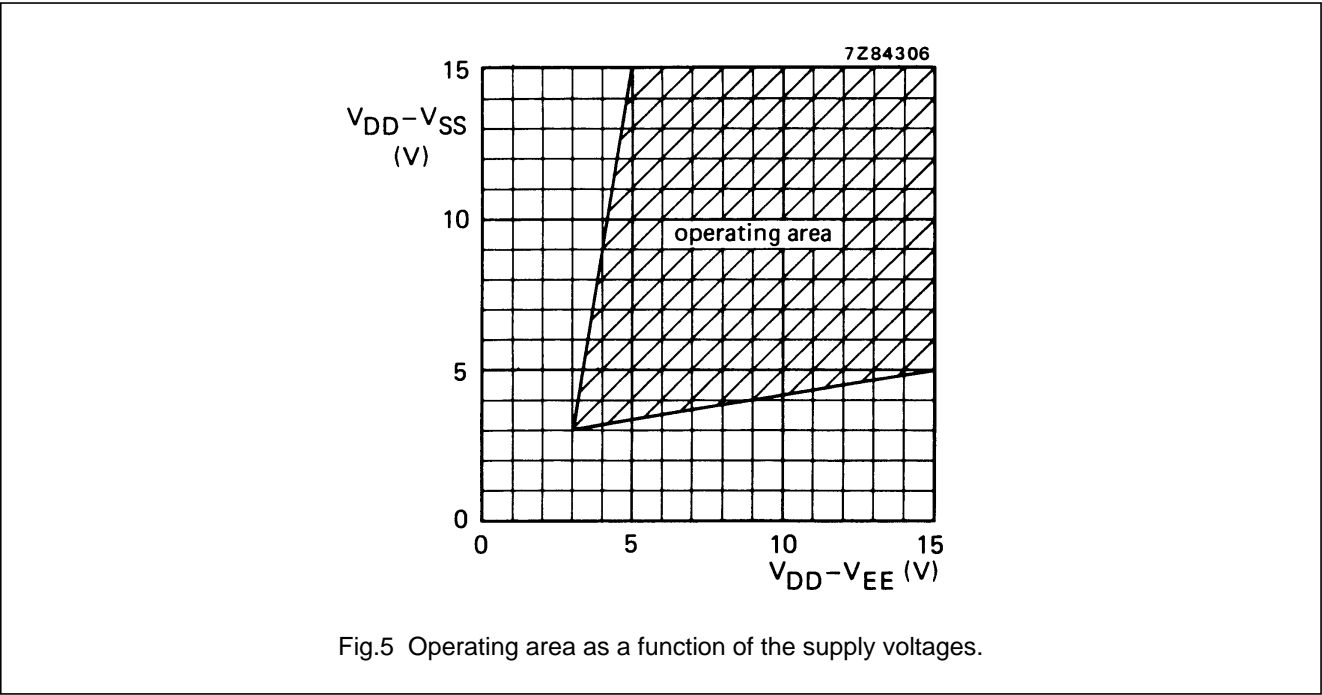


Fig.5 Operating area as a function of the supply voltages.

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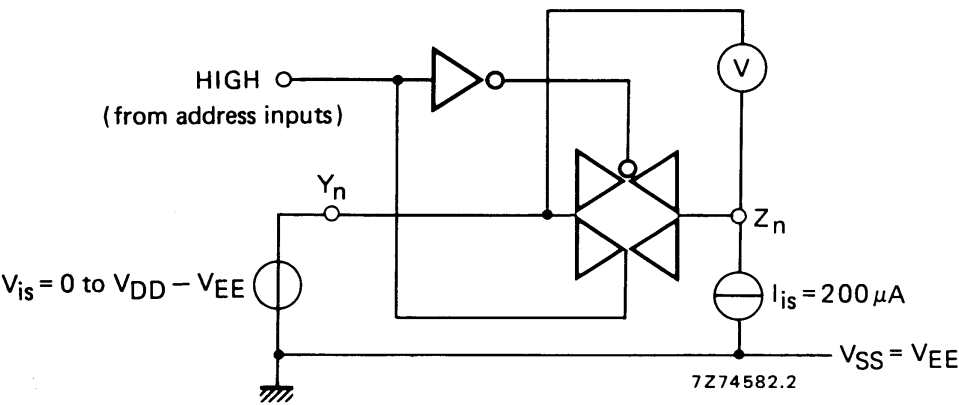


Fig.6 Test set-up for measuring  $R_{ON}$ .

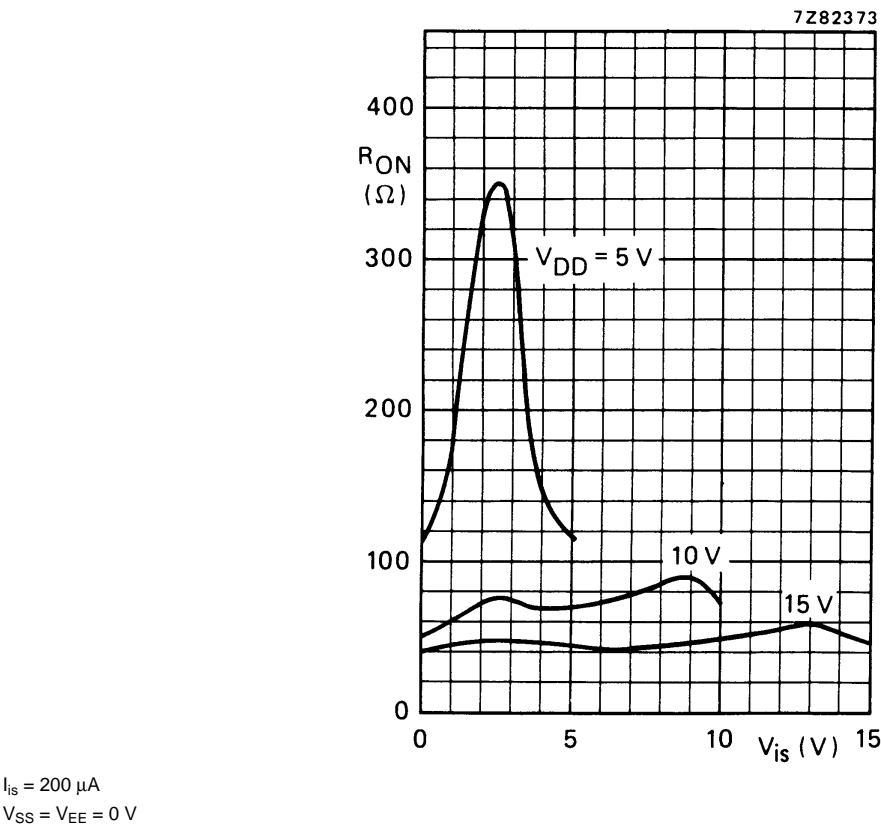


Fig.7 Typical  $R_{ON}$  as a function of input voltage.

## 8-channel analogue multiplexer/demultiplexer

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	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu\text{W}$ )	
Dynamic power dissipation per package (P)	5 10 15	$1\,000\,f_i + \sum(f_o C_L) \times V_{DD}^2$ $5\,500\,f_i + \sum(f_o C_L) \times V_{DD}^2$ $15\,000\,f_i + \sum(f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum(f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)

**AC CHARACTERISTICS** $V_{EE} = V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; input transition times  $\leq 20\text{ ns}$ 

	$V_{DD}$ V	SYMBOL	TYP.	MAX.	
Propagation delays					
$V_{is} \rightarrow V_{os}$	5		15	30	ns
HIGH to LOW	10	$t_{PHL}$	5	10	ns
	15		5	10	ns
LOW to HIGH	5	$t_{PLH}$	15	30	ns
	10		5	10	ns
	15		5	10	ns
$A_n \rightarrow V_{os}$	5		150	300	ns
HIGH to LOW	10	$t_{PHL}$	60	120	ns
	15		45	90	ns
LOW to HIGH	5	$t_{PLH}$	150	300	ns
	10		65	130	ns
	15		45	90	ns
Output disable times					
$\bar{E} \rightarrow V_{os}$	5		120	240	ns
HIGH	10	$t_{PHZ}$	90	180	ns
	15		85	170	ns
LOW	5	$t_{PLZ}$	145	290	ns
	10		120	240	ns
	15		115	230	ns
Output enable times					
$\bar{E} \rightarrow V_{os}$	5		140	280	ns
HIGH	10	$t_{PZH}$	55	110	ns
	15		40	80	ns
LOW	5	$t_{PZL}$	140	280	ns
	10		55	110	ns
	15		40	80	ns

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	$V_{DD}$ V	SYMBOL	TYP.	MAX.	
Distortion, sine-wave response	5 10 15		0,25 0,04 0,04	% % %	note 4
Crosstalk between any two channels	5 10 15		— 1 —	MHz MHz MHz	note 5
Crosstalk; enable or address input to output	5 10 15		— 50 —	mV mV mV	note 6
OFF-state feed-through	5 10 15		— 1 —	MHz MHz MHz	note 7
ON-state frequency response	5 10 15		13 40 70	MHz MHz MHz	note 8

**Notes**

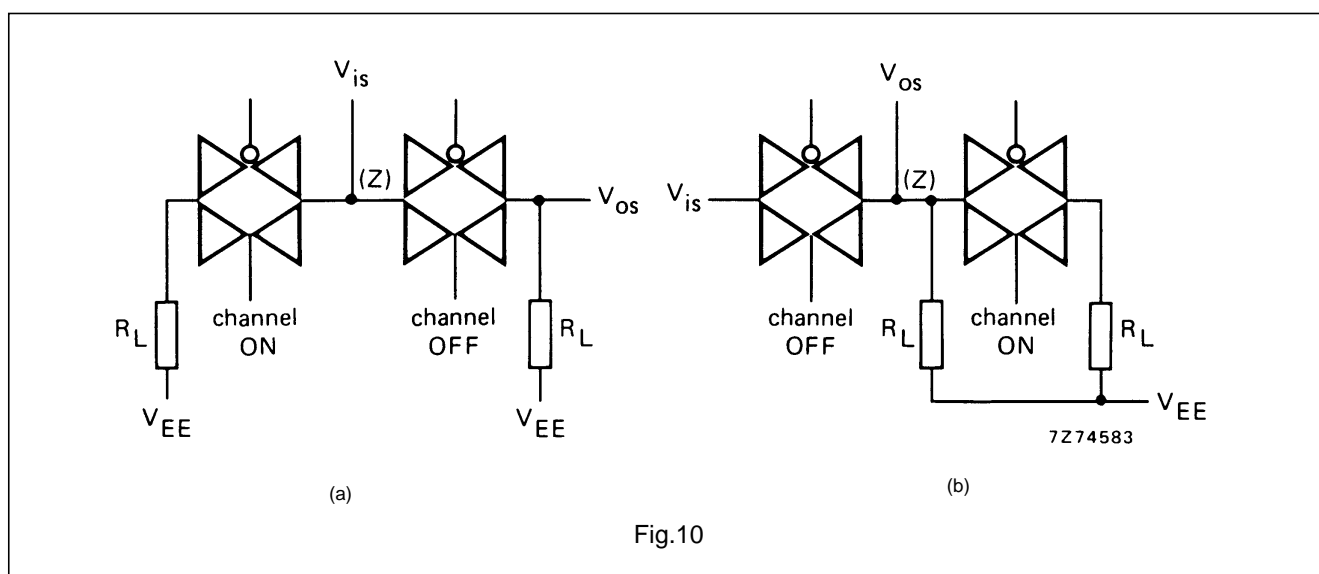
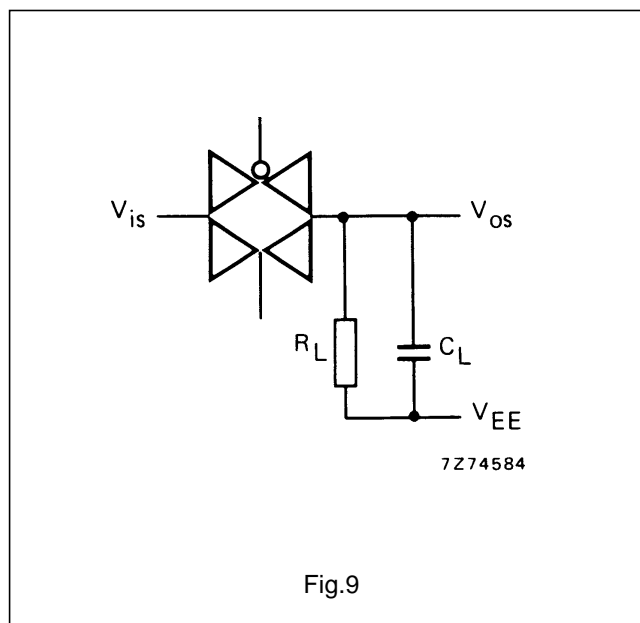
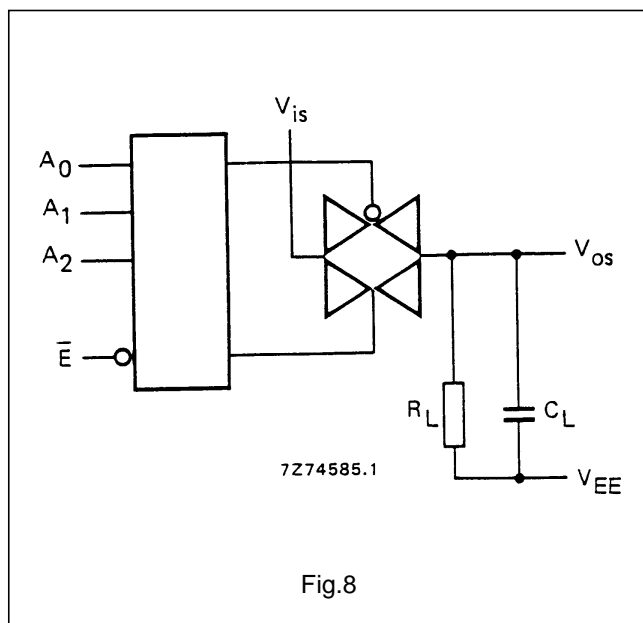
$V_{is}$  is the input voltage at a Y or Z terminal, whichever is assigned as input.

$V_{os}$  is the output voltage at a Y or Z terminal, whichever is assigned as output.

- $R_L = 10\text{ k}\Omega$  to  $V_{EE}$ ;  $C_L = 50\text{ pF}$  to  $V_{EE}$ ;  $\bar{E} = V_{SS}$ ;  $V_{is} = V_{DD}$  (square-wave); see Fig.8.
- $R_L = 10\text{ k}\Omega$ ;  $C_L = 50\text{ pF}$  to  $V_{EE}$ ;  $\bar{E} = V_{SS}$ ;  $A_n = V_{DD}$  (square-wave);  $V_{is} = V_{DD}$  and  $R_L$  to  $V_{EE}$  for  $t_{PLH}$ ;  $V_{is} = V_{EE}$  and  $R_L$  to  $V_{DD}$  for  $t_{PHL}$ ; see Fig.8.
- $R_L = 10\text{ k}\Omega$ ;  $C_L = 50\text{ pF}$  to  $V_{EE}$ ;  $\bar{E} = V_{DD}$  (square-wave);  
 $V_{is} = V_{DD}$  and  $R_L$  to  $V_{EE}$  for  $t_{PHZ}$  and  $t_{PZH}$ ;  
 $V_{is} = V_{EE}$  and  $R_L$  to  $V_{DD}$  for  $t_{PLZ}$  and  $t_{PZL}$ ; see Fig.8.
- $R_L = 10\text{ k}\Omega$ ;  $C_L = 15\text{ pF}$ ; channel ON;  $V_{is} = \frac{1}{2} V_{DD}$  (p-p) (sine-wave, symmetrical about  $\frac{1}{2} V_{DD}$ );  
 $f_{is} = 1\text{ kHz}$ ; see Fig.9.
- $R_L = 1\text{ k}\Omega$ ;  $V_{is} = \frac{1}{2} V_{DD}$  (p-p) (sine-wave, symmetrical about  $\frac{1}{2} V_{DD}$ );  
 $20 \log \frac{V_{os}}{V_{is}} = -50\text{ dB}$ ; see Fig. 10.
- $R_L = 10\text{ k}\Omega$  to  $V_{EE}$ ;  $C_L = 15\text{ pF}$  to  $V_{EE}$ ;  $\bar{E}$  or  $A_n = V_{DD}$  (square-wave); crosstalk is  $|V_{os}|$  (peak value); see Fig.8.
- $R_L = 1\text{ k}\Omega$ ;  $C_L = 5\text{ pF}$ ; channel OFF;  $V_{is} = \frac{1}{2} V_{DD}$  (p-p) (sine-wave, symmetrical about  $\frac{1}{2} V_{DD}$ );  
 $20 \log \frac{V_{os}}{V_{is}} = -50\text{ dB}$ ; see Fig. 9.
- $R_L = 1\text{ k}\Omega$ ;  $C_L = 5\text{ pF}$ ; channel ON;  $V_{is} = \frac{1}{2} V_{DD}$  (p-p) (sine-wave, symmetrical about  $\frac{1}{2} V_{DD}$ );  
 $20 \log \frac{V_{os}}{V_{is}} = -3\text{ dB}$ ; see Fig. 9.



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## APPLICATION INFORMATION

Some examples of applications for the HEF4051B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

## NOTE

If break before make is needed, then it is necessary to use the enable input.

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