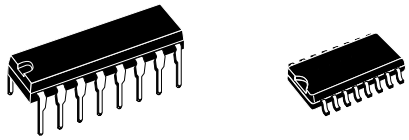
HCF4051

Single 8-channel analog multiplexer/demultiplexer

Datasheet – production data

Features

- Low “ON” resistance: 125 Ω (typ.)
- Over 15 V p.p signal-input range for:
  - V_{DD} - V_{EE} = 15 V
- High “OFF” resistance: channel leakage:
  - ± 100 pA (typ.) at V_{DD} - V_{EE} = 18 V
- Binary address decoding on chip
- High degree of linearity: < 0.5% distortion typ. at f_{IS} = 1 KHz, V_{IS} = 5 V_{pp}, V_{DD} - $V_{SS} \geq$ 10 V, R_L = 10 KΩ
- Very low quiescent power dissipation under all digital control input and supply conditions:
  - 0.2 µW (typ.) V_{DD} - V_{SS} = V_{DD} - V_{EE} = 10 V
- Matched switch characteristics:
  - R_{ON} = 5 Ω (typ.) for V_{DD} - V_{EE} = 15 V
- Wide range of digital and analog signal levels: digital 3 to 20, analog to 20 V p.p.
- Quiescent current specified up to 20 V
- 5 V, 10 V and 15 V parametric ratings
- Input leakage current I_I = 100 nA (max.) at:
  - V_{DD} = 18 V, T_A = 25 °C
- 100% tested for quiescent current
- Meets all requirements of JEDEC JESD13B “Standard specifications for description of B series CMOS devices”
- ESD performance
  - HBM: 2000 V
  - MM: 200 V
  - CDM: 1000 V



PDIP16 SO16

Applications

- Automotive
- Industrial
- Computer
- Consumer

Figure 1. Pin connection

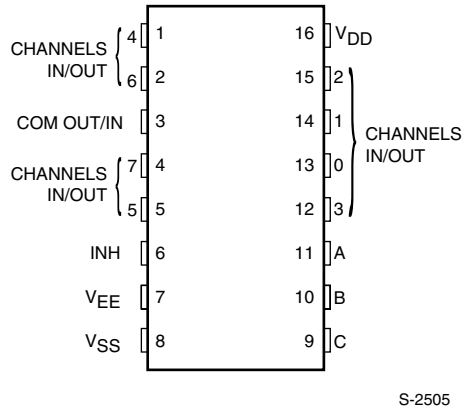


Table 1. Device summary

Order code	Temperature range	Package	Packaging	Marking
HCF4051M013TR	-55/+125 °C	SO16	Tape and reel	HCF4051
HCF4051YM013TR(1)	-40/+125 °C	SO16 (automotive version)	Tape and reel	HCF4051Y
HCF4051BEY	-55/+125 °C	PDIP16	Tube	HCF4051BE

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.

1 Description

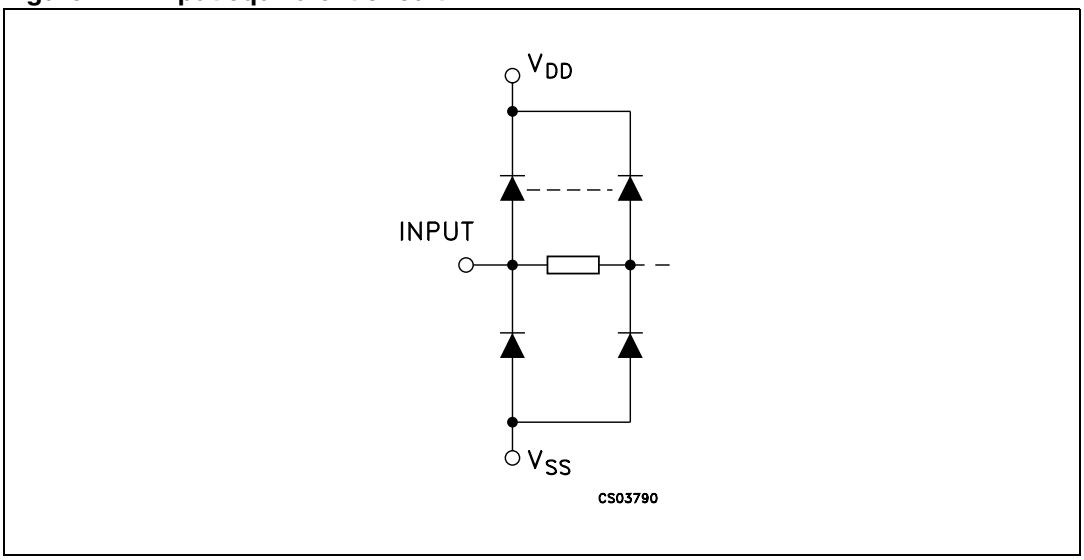
The HCF4051 device is a monolithic integrated circuit fabricated in MOS (metal oxide semiconductor) technology available in SO16 and PDIP16 packages.

The HCF4051 analog multiplexer/demultiplexer is a digitally controlled analog switch having low ON impedance and very low OFF leakage current. This multiplexer circuit dissipate extremely low quiescent power over the full $_{VDD}$ - V_{SS} and V_{DD} - V_{EE} supply voltage range, independent of the logic state of the control signals.

When a logic “1” is present at the inhibit input terminal all channel are off. This device is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

2 Input equivalent circuit

Figure 2. Input equivalent circuit



3 Pin settings

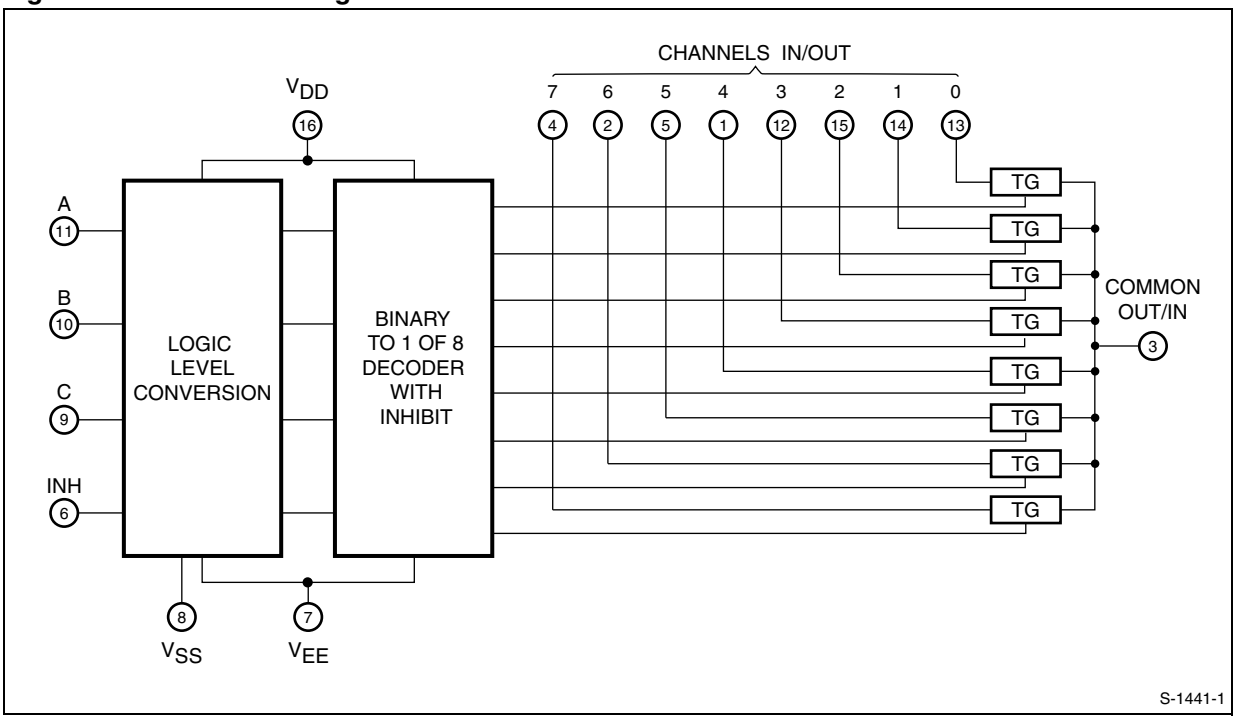
Table 2. Pin description

Pin no.	Symbol	Name and function
11, 10, 9	A, B, C	Binary control inputs
6	INH	Inhibit inputs
13, 14, 15, 12, 1, 5, 2, 4	0 to 7 channel IN/OUT	Independent inputs/outputs
3	COM OUT/IN	Common output/input
7	V_{EE}	Supply voltage
8	V_{SS}	Negative supply voltage
16	V_{DD}	Positive supply voltage

Table 3. Truth table

Input states				"ON" channel (S)
Inhibit	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None

Figure 3. Functional diagram



4 Maximum ratings

Table 4. Absolute maximum ratings(1), (2)

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.5 to +22	V
V_I	DC input voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC input current	±10	mA
P_D	Power dissipation per package	500(3)	mW
	Power dissipation per output transistor	100	mW
T_{op}	Operating temperature	-55 to +125	°C
T_{stg}	Storage temperature	-65 to +150	°C

1. Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
2. All voltage values are referred to V_{SS} pin voltage.
3. 500 mW at 65 °C; derate to 300 mW by 10 mW/°C from 65 °C to 85 °C.

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	3 to 20	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature	-55 to 125	°C

5 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	Test condition				Value					Unit
		V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	T_A = 25 °C			-55 to 125 °C		
						Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent device current (all switches ON or all switches OFF)				5		0.04	5		150	µA
					10		0.04	10		300	
					15		0.04	20		600	
					20		0.08	100		3000	
Switch											
R_{ON}	Resistance	$0 \le V_I \le V_{DD}$	0	0	5		470	1050		1200	Ω
					10		180	400		520	
					15		125	280		360	
D_{ON}	Resistance Δ_{RON} (between any 2 of 4 switches)	$0 \le V_I \le V_{DD}$	0	0	5		10				Ω
					10		10				
					15		5				
OFF(1)	Channel leakage current (all channels OFF) (COMMON O/I)		0	0	18		±0.1	100		1000	nA
OFF(1)	Channel leakage current (any channel OFF)		0	0	18		±0.1	100		1000	nA
C_I	Input capacitance		-5	-5	5		5				pF
C_O	Output capacitance						30				
C_{IO}	Feedthrough						0.2				
Control (address or inhibit)											
V_{IL}	Input low voltage	= V_{DD} thru 1 KΩ	V_{EE} = V_{SS} R_L = 1KΩ to V_{SS} I_{IS} < 2µA (on all OFF channels)		5			1.5		1.5	V
					10			3		3	
					15			4		4	
V_{IH}	Input high voltage				5	3.5			3.5		V
					10	7			7		
					15	11			11		
I_{IH}, I_{IL}	Input leakage current	V_I = 0/18 V			18		$\pm 10^{-3}$	±0.1		±1	µA
C_I	Input capacitance						5	7.5			pF

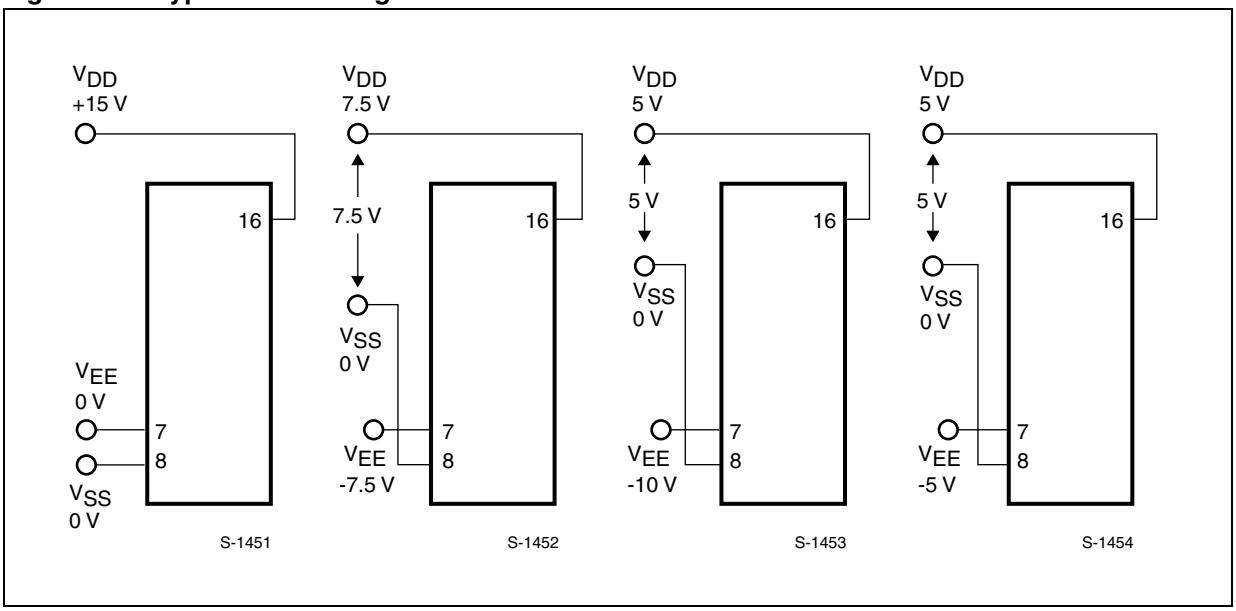
1. Determined by minimum feasible leakage measurement for automating testing.

Table 7. Dynamic electrical characteristics (T_{amb} = 25 °C, C_L = 50 pF, all input square wave rise and fall time = 20 ns)(1)

Parameter	Test condition							Value			Unit
	V_{EE} (V)	R_L (KΩ)	f_I (KHz)	V_I (V)	V_{SS} (V)	V_{DD} (V)		Min.	Typ.	Max.	
Propagation delay time (signal input to output)		200		V_{DD}		5			30	60	ns
						10			15	30	
						15			11	20	
Frequency response channel "ON" (sine wave input) at 20 log V_O/V_I = -3 dB	= V_{SS}	1		5(2)		10	V_O at common OUT/IN		20		MHz
							V_O at any channel		60		
Feedthrough (all channels OFF) at 20 log V_O/V_I = - 40 dB	= V_{SS}	1		5(2)		10	V_O at common OUT/IN		12		MHz
							V_O at any channel		8		
Frequency signal crosstalk at 20 log V_O/V_I = -40 dB	= V_{SS}	1		5(2)		10	Between any 2 channels		3		MHz
Sine wave distortion f_{IS} = 1 KHz sine wave	= V_{SS}	10	1	2(2)		5			0.3		%
				3(2)		10			0.2		
				5(2)		15			0.12		
Control (address or inhibit)											
Propagation delay: address to signal OUT (channels ON or OFF)	0				0	5			360	720	ns
	0				0	10			160	320	
	0				0	15			120	240	
	-5				0	5			225	450	
Propagation delay: inhibit to signal OUT (channel turning ON)	0	1			0	5			360	720	ns
	0				0	10			160	320	
	0				0	15			120	240	
	-10				0	5			200	400	
Propagation delay: inhibit to signal OUT (channel turning OFF)	0	10				5			200	450	ns
	0					10			90	210	
	0					15			70	160	
	-10					5			130	300	
Address or inhibit to signal crosstalk	0	10 (1)			0	10	$V_C = V_{DD} - V_{SS}$ (square wave)		65		mV peak

1. Both ends of channel.
2. Peak-to-peak voltage symmetrical about (V_{DD} - V_{EE}) /2.

Figure 4. Typical bias voltages



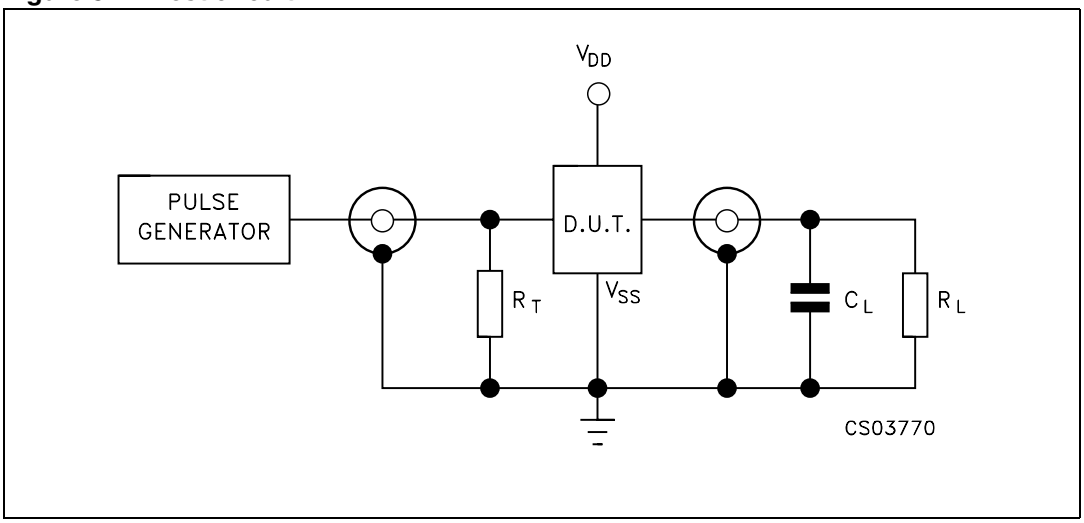
1. The ADDRESS (digital-control inputs) and INHIBIT logic levels are : “0” = V_{SS} and “1” = V_{DD}. The analog signal (through the TG) may swing from V_{EE} to V_{DD}.

Special considerations

Control of analog signals up to 20 V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20 V (if V_{DD} - V_{SS} = 3 V, a V_{DD} - V_{EE} of up to 13 V can be controlled; for V_{DD} - V_{EE} level differences above 13 V, a V_{DD} - V_{SS} of at least 4.5 V is required. For example, if V_{DD} = +5, V_{SS} = 0, and V_{EE} = -13.5, analog signals from -13.5 V to 4.5 V can be controlled by digital inputs of 0 to 4.5 V. In certain applications, the external load resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 V (calculated from R_{ON} values shown in *Table 6: DC specifications*). No V_{DD} current will flow through R_L if the switch current flows into lead 3.

6 Test circuit

Figure 5. Test circuit



1. C_L = 50 pF or equivalent (includes jig and probe capacitance)
   R_L = 200 KΩ
   $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω).

7 Waveforms

Figure 6. Waveform 1: channel being turned ON (R_L = 1 KΩ, f = 1 MHz; 50% duty cycle)

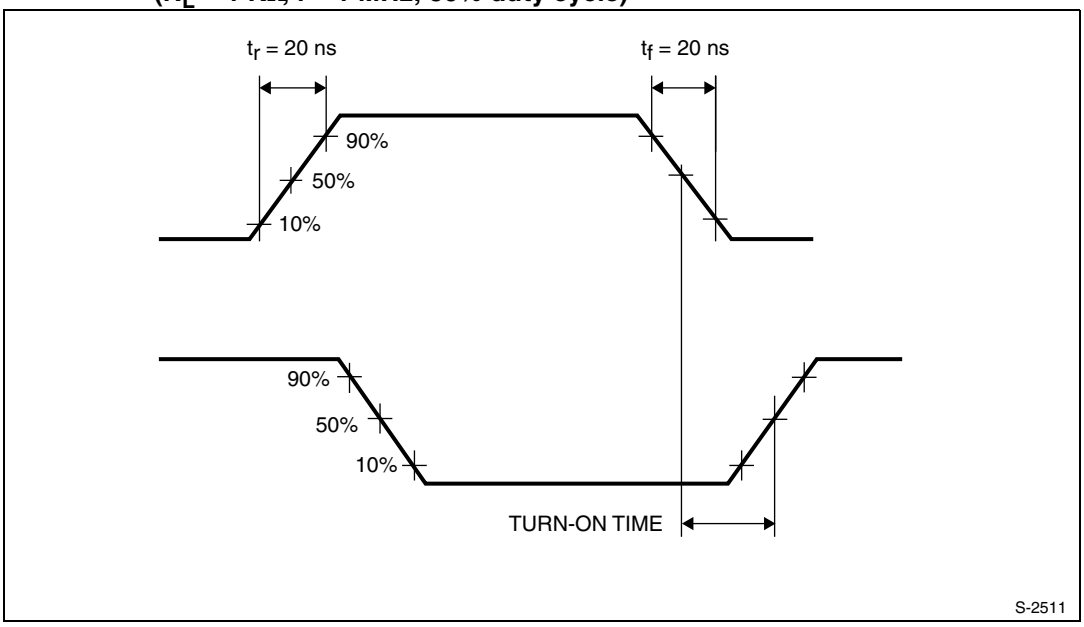
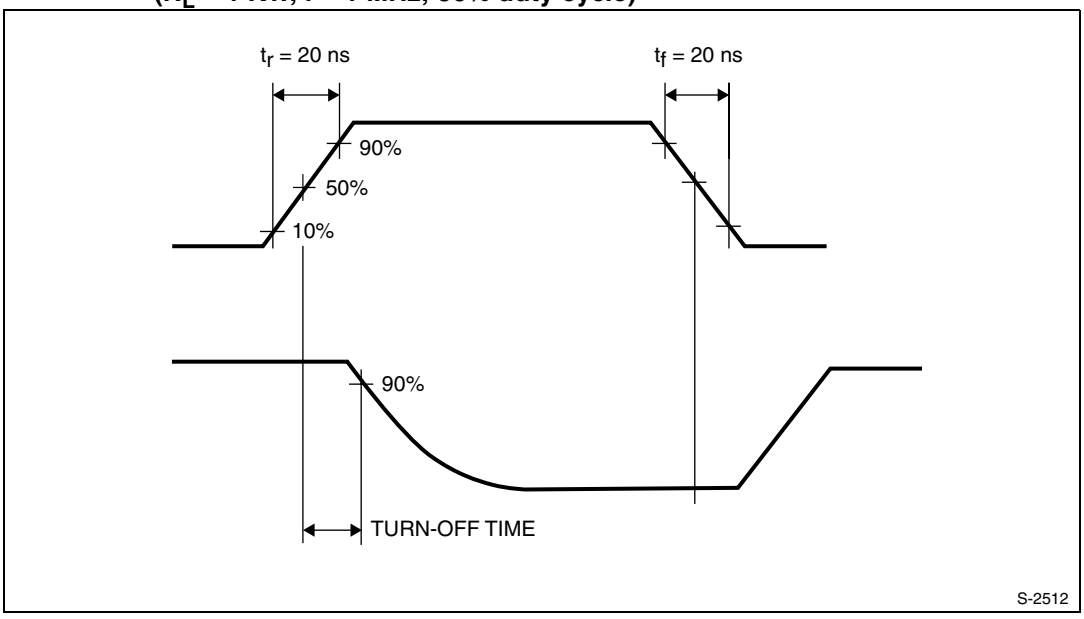


Figure 7. Waveform 2: channel being turned OFF (R_L = 1 KW, f = 1 MHz; 50% duty cycle)



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 8. Plastic PDIP16 (0.25) package outline

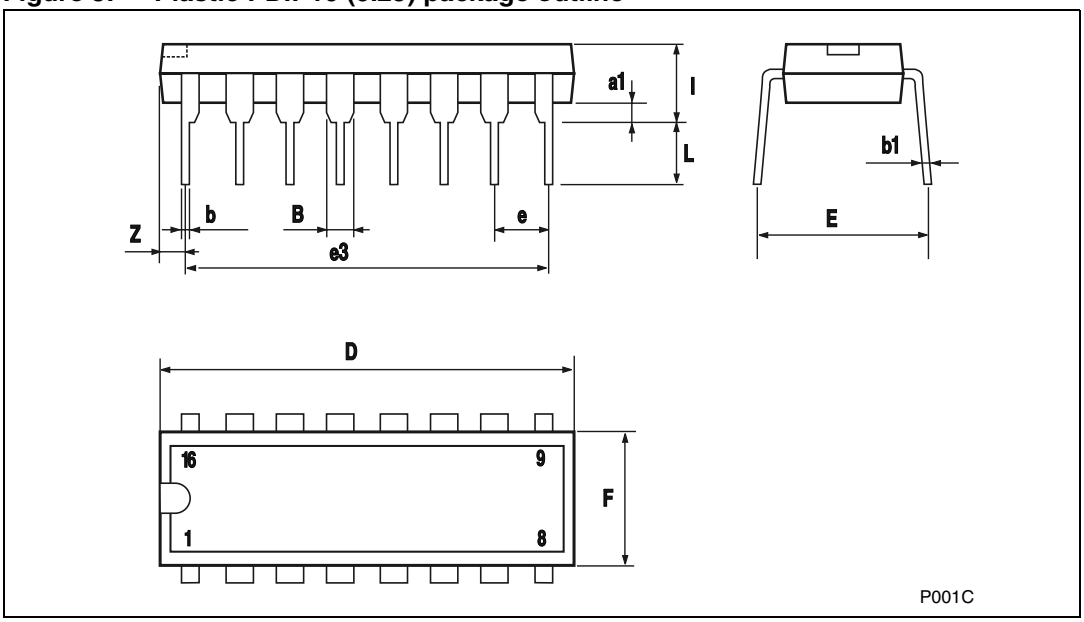


Table 8. Plastic PDIP16 (0.25) package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

Figure 9. SO16 package outline

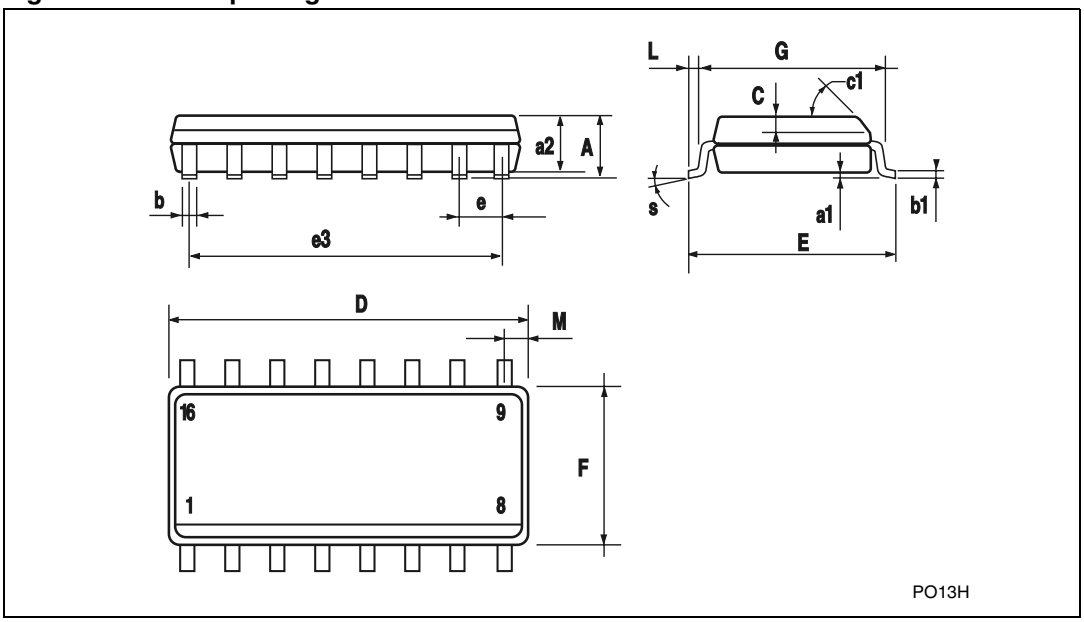


Table 9. SO16 package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 ° (max.)					

9 Revision history

Table 10. Document revision history

Date	Revision	Changes
26-Oct-2012	2	Updated *Features* (added ESD values), added *Applications*. Updated *Table 1* (reformatted table, added order codes, temperature range, marking, updated package and packaging). Updated *Description* (unified part numbers, moved to page 2). Updated *Section 2* to *Section 8* (added titles and numbering). Updated *Table 6* (removed -40/+85° temperature range). Reformatted *Section 8* (added ECOPACK text, *Figure 8*, *Figure 9*, *Table 8*, and *Table 9*). Minor corrections throughout document.

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