PRODUCT DEVELOPMENT

(DEPARTMENT)

MODULE : GF5035TNWBZNL04 **(G64128W07NBW00)**

TYPE OF TEST : COG

	Designation	Name	Signature/Date
Originator	**ELECTRONIC ENGINEER**	**NOR AZLINA MUSLIM**	
Reviewed by	**ASST. MANAGER SOFTWARE**	**ZAINUL AZHAN AHMAD BASHIR**	
Approved by	**HOD PROD. DEV. LCM**	**VUTHY TAING**	

1.0 TABLE OF CONTENTS

2.0 RECORD OF DIVISION

Rev	Date	Item	Page	Comment
A	9/11/04			Initial Release

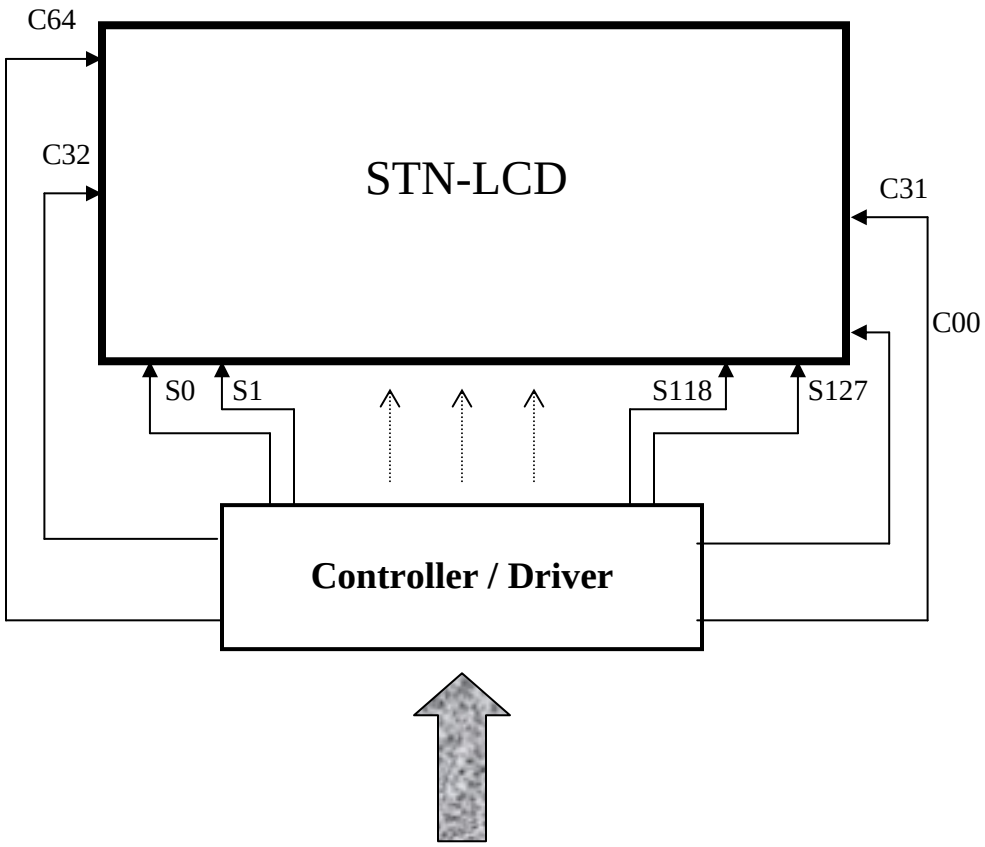
3.0 General Specifications

- **Display format: 128 * 64 dot matrix graphic**
- **Microprocessor interface: Parallel/Serial**
- **LCD type: FSTN Negative Dark Blue**
- **Viewing angle: 6 o'clock**
- **LCD controller: S1D10605D04B**
- **VDD: 2.7V (Min), 3.3V (Max)**
- **Operating temperature: -20°C to 70°C**
- **Storage temperature: -30°C to 80°C**
- **Front polarizer: Transmissive**
- **Back polarizer: Transmissive**
- **Pin outs connection: FFC**
- **Module size: 76.00 x 50.60 mm**
- **View area: 70.70 x 38.80 mm**
- **Active area: 66.52 x 33.24 mm**
- **Dot size: 0.48 x 0.48 mm**
- **Dot pitch: 0.52 x 0.52 mm**
- **Driving method: 1/64 duty, 1/9 bias**
- **Backlight: White ; Vf:4.0V ; If:60mA**

4.0 DEFINITIONS OF TERMINALS

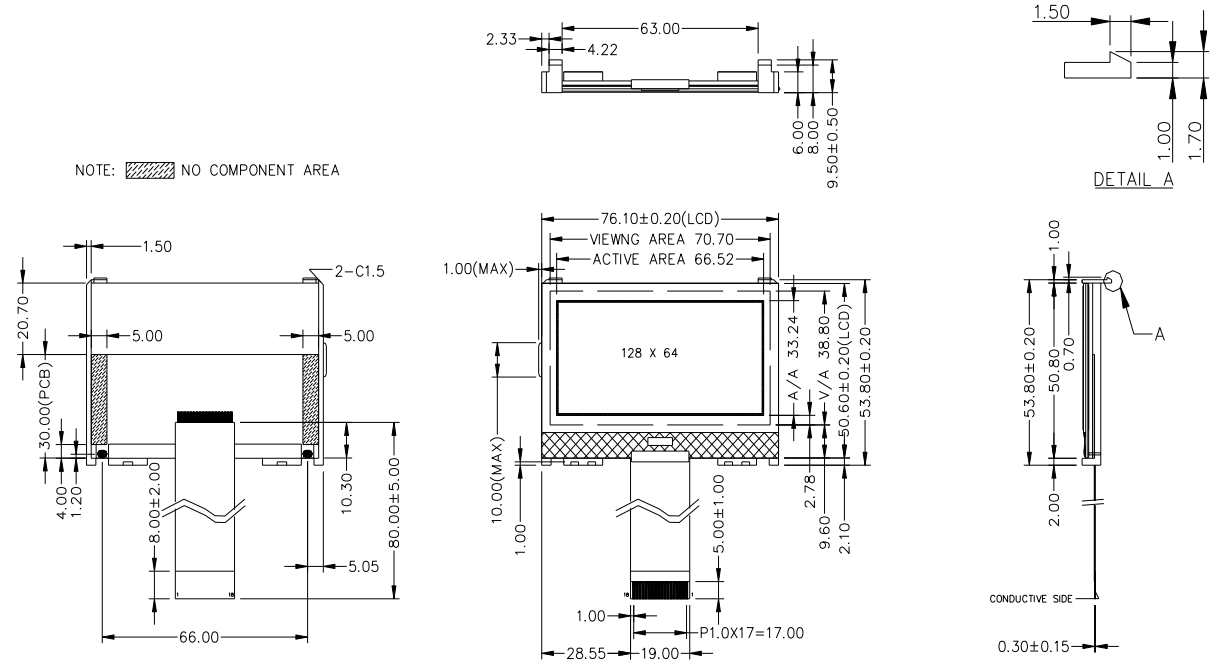
Pin No.	Symbol	Function
1	Vss	Ground
2	Vdd	Logic Power Supply
3	Vout	Booster Output Voltage
4	RES	Reset Terminal
5	CS	Chip Select Terminal
6	RS	Data or Command Terminal
7	R/W	Read / Write Terminal
8	E	Enable Terminal
9	DB0	Data Line Terminal
10	DB1	Data Line Terminal
11	DB2	Data Line Terminal
12	DB3	Data Line Terminal
13	DB4	Data Line Terminal
14	DB5	Data Line Terminal
15	DB6	Data Line Terminal
16	DB7	Data Line Terminal
17	Anode	Backlight Anode Terminal
18	Cathode	Backlight Cathode Terminal

5.0 BLOCK DIAGRAM



6.0 MECHANICAL SPECIFICATIONS

Glass Overall View

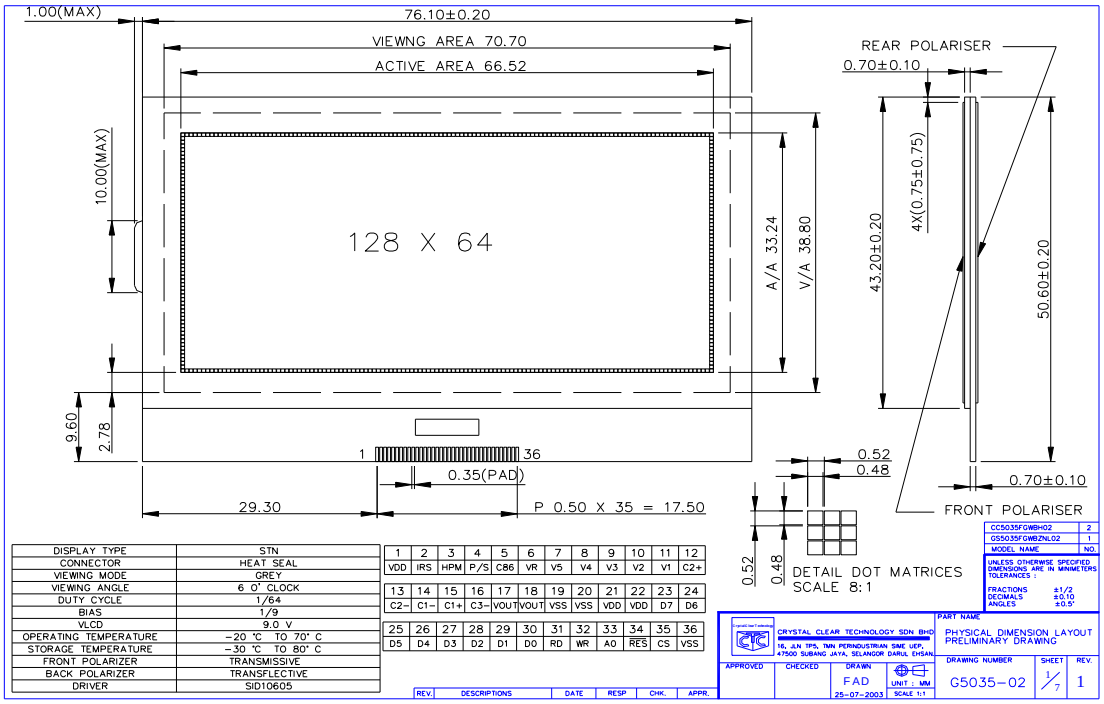


PIN ASSIGNMENT

PIN	1	2	3	4	5	6	7	8	9
SYMBOL	V_{SS}	V_{DD}	V_o	$\overline{RES}$	$\overline{CS}$	RS	R/W	E	DB0

PIN	10	11	12	13	14	15	16	17	18
SYMBOL	DB1	DB2	DB3	DB4	DB5	DB6	DB7	A	K

Glass Drawing



DISPLAY TYPE	STN
CONNECTOR	HEAT SEAL
VIEWING MODE	GREY
VIEWING ANGLE	6 O' CLOCK
DUTY CYCLE	1/64
BIAS	1/9
VLCD	9.0 V
OPERATING TEMPERATURE	−20 °C TO 70° C
STORAGE TEMPERATURE	−30 °C TO 80° C
FRONT POLARIZER	TRANSMISSIVE
BACK POLARIZER	TRANSFLECTIVE
DRIVER	SID10605

1	2	3	4	5	6	7	8	9	10	11	12
VDD	IRS	HPM	P/S	C86	VR	V5	V4	V3	V2	V1	C2+

13	14	15	16	17	18	19	20	21	22	23	24
C2−	C1−	C1+	C3−	VOUT	VOUT	VSS	VSS	VDD	VDD	D7	D6

25	26	27	28	29	30	31	32	33	34	35	36
D5	D4	D3	D2	D1	D0	RD	WR	A0	$\overline{RES}$	CS	VSS

REV.	DESCRIPTIONS	DATE	RESP	CHK.	APPR.

CC5035FGWBH02	2
GS5035FGWBZNL02	1
MODEL NAME	NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS
TOLERANCES :
FRACTIONS ±1/2
DECIMALS ±0.10
ANGLES ±0.5°

CRYSTAL CLEAR TECHNOLOGY SDN BHD
NO. 4,JLN TPP5, TMN PERINDUSTRIAN SME UEP,
47500 SUBANG JAYA, SELANGOR DARUL EHSAN

PART NAME: PHYSICAL DIMENSION LAYOUT
PRELIMINARY DRAWING

APPROVED	CHECKED	DRAWN	UNIT : MM	DRAWING NUMBER	SHEET	REV.
		FAD 25-07-2003	SCALE 1:1	G5035-02	1/7	1

7.0 POWER SUPPLY CIRCUITS

As this model was built in master mode then it is possible to control power consumption for liquid crystal drive. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. Table below shows the referenced combinations in using power supply circuits.

The Control Details of Each Bit of the Power Control Set Command

Item	Status "1"	Status "0"
D2 Booster circuit control bit	ON	OFF
D1 Voltage regulator circuit (V regulator circuit) control bit	ON	OFF
D0 Voltage follower circuit (V/F circuit) control bit	ON	OFF

Use Settings	D2	D1	D0	Step-up circuit	V regulator circuit	V/F circuit	External voltage input	Step-up voltage system terminal
① Only the internal power supply is used	1	1	1	O	O	O	V_{SS2}	Used
② Only the V regulator circuit and the V/F circuit are used	0	1	1	X	O	O	V_{OUT}, V_{SS2}	Open
③ Only the V/F circuit is used	0	0	1	X	X	O	V_5, V_{SS2}	Open
④ Only the external power supply is used	0	0	0	X	X	X	V_1 to V_5	Open

* The "step-up system terminals" refer CAP1+, CAP1–, CAP2+, CAP2–, and CAP3–.
* While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

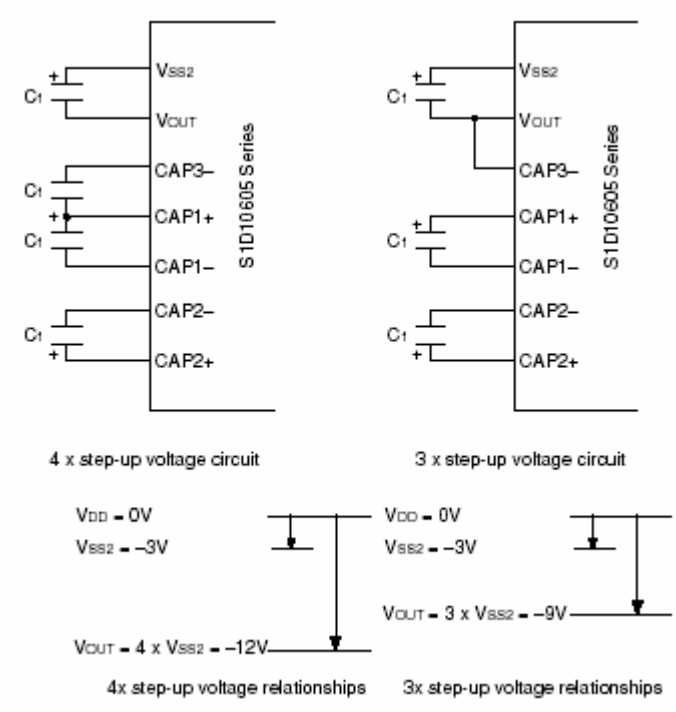
The Step-up Voltage Circuits

Using the step-up voltage circuits equipped within the module chips it is possible to product a Triple step-up, and a Double step-up of the VDD – VSS2 voltage levels.

• Quad step-up: Connect capacitor C1 between CAP1+and CAP1–, between CAP2+ and CAP2–, between CAP1+ and CAP3–, and betweenVSS2 and VOUT, to produce a voltage level in the negative direction at the VOUT terminal that is 4 times the voltage level between VDD and VSS2.

• Triple step-up: Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2– and between VSS2 and VOUT, and short between CAP3– and VOUT to produce a voltage level in the negative direction at the VOUT terminal that is 3 times the voltage difference between VDD and VSS2.

Reference Circuits



*** The VSS2 voltage range must be set so that the VOUT terminal voltage does not exceed the absolute maximum rated value.**

(4-Time V/C:ON, V/R:ON, V/F:ON)

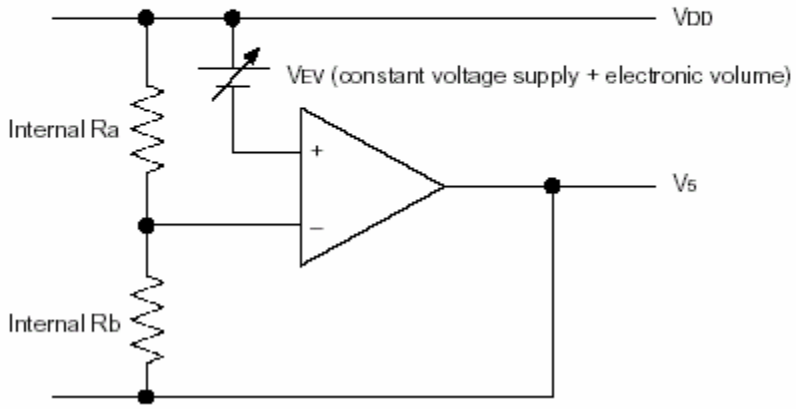
The Voltage Regulator Circuit

The step-up voltage generated at VOUT outputs the liquid crystal driver voltage V5 through the voltage regulator circuit. Because the module driver chip have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V5 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components. The selected thermal gradients Vreg approximately 0.05%

When the V5 Voltage Regulator Internal Resistors Are Used

Through the use of the V5 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V5 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V5 voltage can be calculated using equation A-1 over the range where | V5 | < | VOUT |.

$$V_5 = \left(1+\frac{Rb}{Ra}\right)\cdot V_{EV}$$
$$= \left(1+\frac{Rb}{Ra}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG}$$
$$\left[\because V_{EV} = \left(1-\alpha/162\right)\cdot V_{REG}\right] \qquad \text{(Equation A-1)}$$



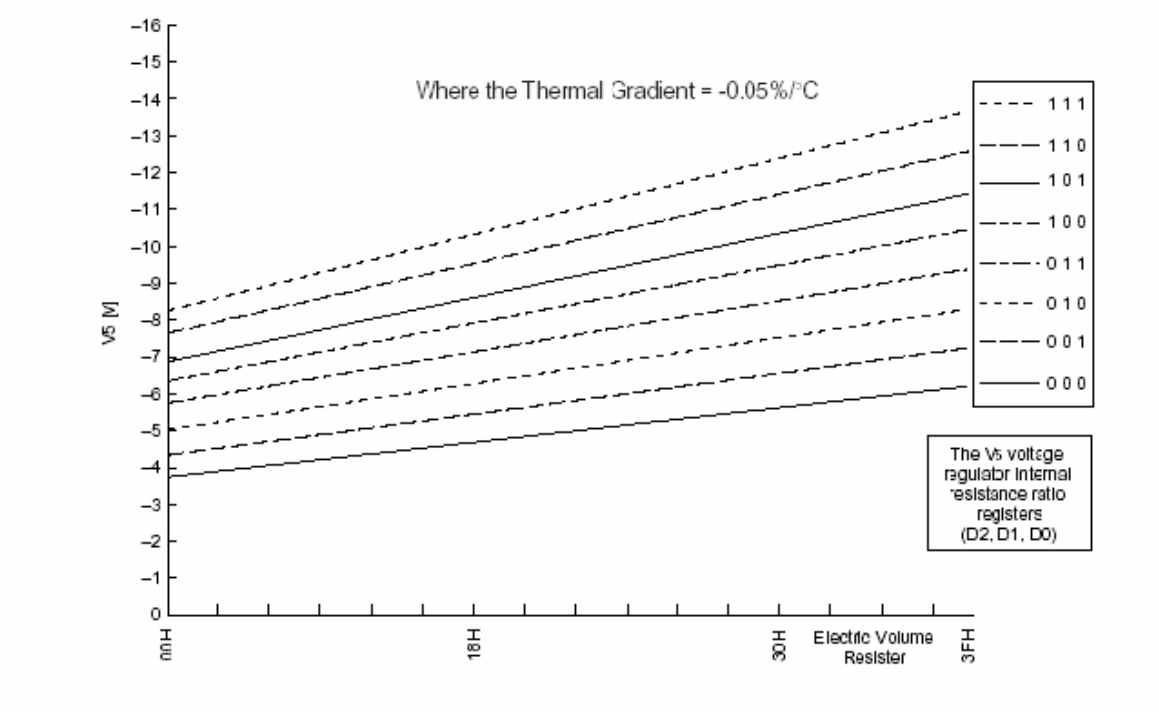
Equipment Type	Thermal Gradient	Units	VREG	Units
Internal Power Supply	–0.05	[%/°C]	–2.1	[V]

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 4 shows the value for α depending on the electronic volume register settings.

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
			⋮			⋮
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

Rb/Ra is the V5 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V5 voltage regulator internal resistor ratio set command. The (1 + Rb/Ra) ratio assumes the values shown in Table 5 depending on the 3-bit data settings in the V5 voltage regulator internal resistor ratio register.

Register			Equipment Type by Thermal Gradient [Units: %/°C]	
D2	D1	D0	–0.05	VREG External Input
0	0	0	3.0	1.5
0	0	1	3.5	2.0
0	1	0	4.0	2.5
0	1	1	4.5	3.0
1	0	0	5.0	3.5
1	0	1	5.4	4.0
1	1	0	5.9	4.5
1	1	1	6.4	5.0



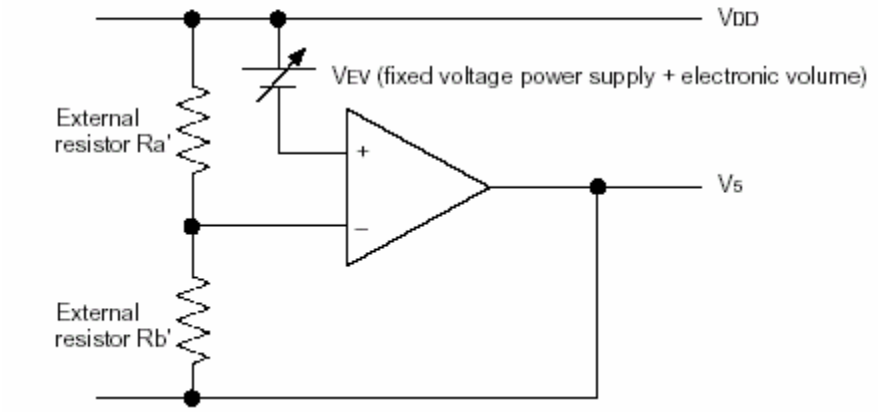
The Vs votage as a function of the Vs votage regulatcr internal resistor ratio register and the electronic volume register.

When an External Resistance is Used (i.e., The V5 Voltage Regulator Internal Resistors Are Not Used)

The liquid crystal power supply voltage V5 can also be set without using the V5 voltage regulator internal resistors (IRS terminal = LOW) by adding resistors Ra' and Rb' between VDD and VR, and between VR and V5, respectively. When this is done, the use of the electronic volume function makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal power supply voltage V5 through commands. In the range where | V5 | < | VOUT |, the V5 voltage can be calculated using equation B-1 based on the external resistances Ra' and Rb'.

Setup example: When selecting Ta = 25 C and V5 = –7 V for the LCD module where the temperature gradient = –0.05%/°C.

$$V_5 = \left(1+\frac{Rb'}{Ra'}\right)\cdot V_{EV}$$
$$= \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG}$$
$$\left[\because V_{EV} = \left(1-\frac{\alpha}{162}\right)\cdot V_{REG}\right] \quad \text{(Equation B-1)}$$



When the central value of the electron volume register is (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), then $\alpha = 31$ **and VREG = –2.1 V so, according to equation B-1,**

$$V_5 = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG}$$
$$-11V = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{31}{162}\right)\cdot(-2.1) \quad \text{(Equation B-2)}$$

Moreover, when the value of the current running through Ra' and Rb' is set to 5 μA,

$Ra\ Rb\ M'\ '\ .\ +\ =1\ 4\ \Omega$ (Equation B-3)

Consequently, by equations B-2 and B-3,

$$\frac{Rb'}{Ra'} = 3.12$$
$$Ra' = 340k\Omega$$
$$Rb' = 1060k\Omega$$

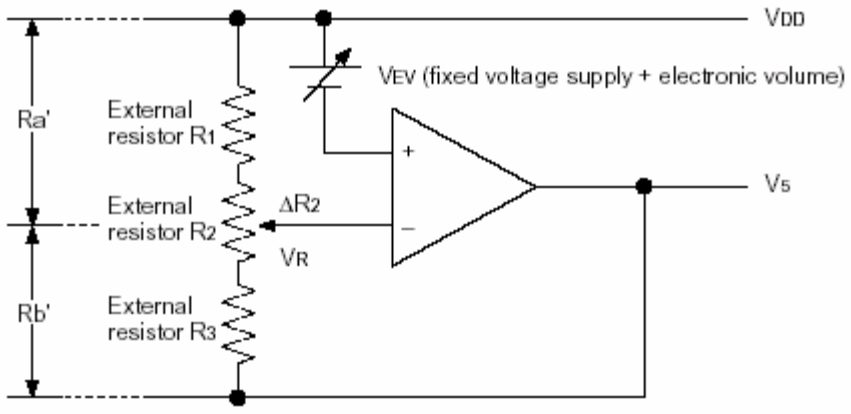
At this time, the V5 voltage variable range and notch width, based on the electron volume function, is as given in Table 6.

V5	Min.	Typ.	Max.	Units
Variable Range Notch width	–8.6 (63 levels)	–7.0 (central value) 52	–5.3 (0 level)	[V] [mV]

When External Resistors are Used (i.e. The V5 Voltage Regulator Internal Resistors Are Not Used).

When the external resistor described above are used, adding a variable resistor as well makes it possible to perform fine adjustments on Ra' and Rb', to set the liquid crystal drive voltage V5. In this case, the use of the electronic volume function makes it possible to control the liquid crystal power supply voltage V5 by commands to adjust the liquid crystal display brightness. In the range where | V5| < | VOUT | the V5 voltage can be calculated by equation C-1 below based on the R1 and R2 (variable resistor) and R3 settings, where R2 can be subjected to fine adjustments (Δ R2)**..**

$$V_5 = \left(1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right) \cdot V_{EV}$$
$$= \left(1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}$$
$$\because V_{EV} = \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}\Big] \qquad \text{(Equation C-1)}$$



Setup example: When selecting Ta = 25°C and V5 = – 5 to –9 V (using R2) for the module where the temperature gradient = –0.05%/°C.

When the central value for the electronic volume register is set at (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0),

α =**31**
$V_{REG} = -2.1\ V$.

so, according to equation C-1, when $\Delta R2 = 0\ \Omega$, **in order to make V5 = –9 V**,

$$-9V = \left(1 + \frac{R_3 + R_2}{R_1}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (-2.1)$$

(Equation C-2)

$$-5V = \left(1 + \frac{R_3}{R_1 + R_2}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (-2.1)$$

(Equation C-3)

When $\Delta R2 = R2$, **in order to make V = –5 V,**

$$-5V = \left(1 + \frac{R_3}{R_1 + R_2}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (-2.1)$$

(Equation C-3)

Moreover, when the current flowing VDD and V5 is set to 5 μ**A,**

$$R_1 + R_2 + R_3 = 1.4M\Omega \qquad \text{(Equation C-4)}$$

With this, according to equation C-2, C-3 and C-4,

$$R_1 = 264k\Omega$$
$$R_2 = 211k\Omega$$
$$R_3 = 925k\Omega$$

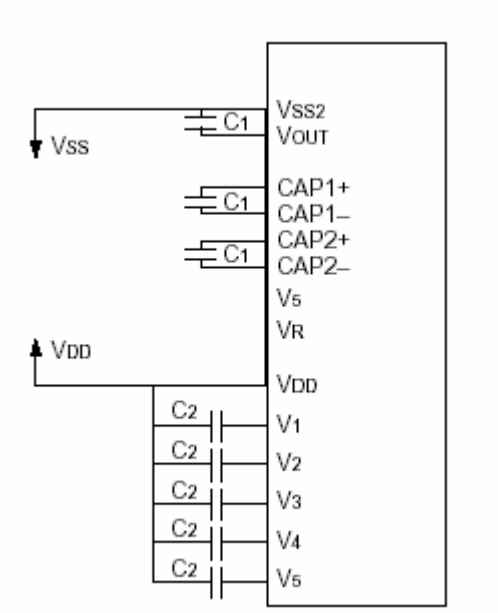
At this time, the V5 voltage variable range and notch width based on the electron volume function is as shown in Table 7.

V_5	Min.	Typ.	Max.	Units
Variable Range	–8.7 (63 levels)	–7.0 (central value)	–5.3 (0 level)	[V]
Notch width		53		[mV]

Reference Circuits

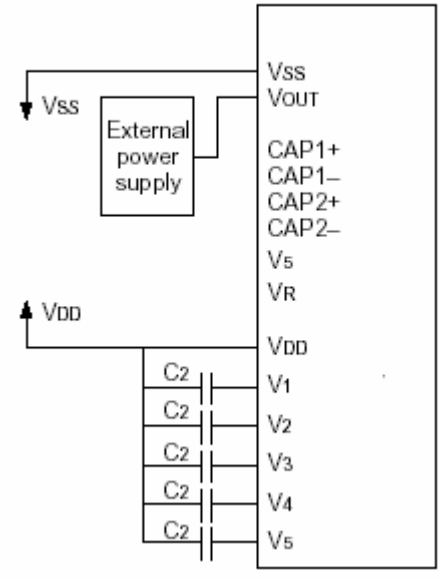
When used all of the step-up circuit, voltage regulating circuit and V/F circuit

When the voltage regulator internal resistor is used. (Example where VSS2 = VSS, with 3x step-up)



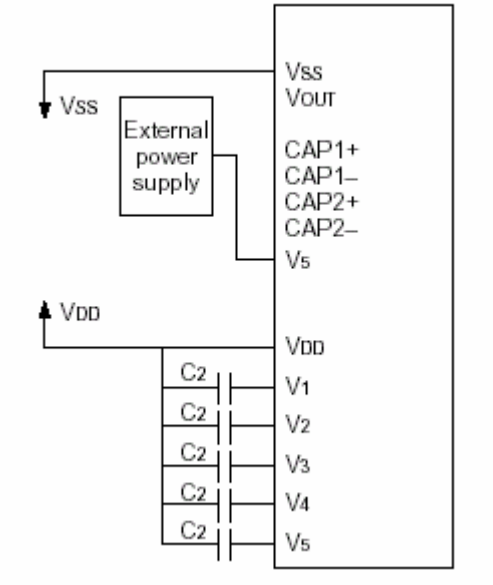
When the voltage regulator circuit and V/F circuit alone are used

When the V5 voltage regulator internal resistor is used.

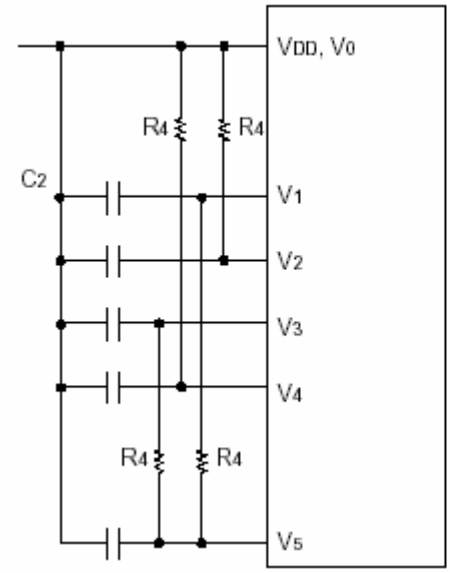


When the V/F circuit alone is used

Examples of shared reference settings, When V5 can vary between –8 and 12 V



When the built-in power circuit is used to drive a liquid crystal panel heavily loaded with AC or DC, it is recommended to connect an external resistor to stabilize potentials of V1, V2, V3 and V4 which are output from the built-in voltage follower.



Reference set value R4: 100kΩ ~ 1MΩ
It is recommended to set an optimum resistance value R4 taking the liquid crystal display and the drive waveform.

Item	Set value	Units
C1	1.0 to 4.7	µF
C2	0.01 to 1.0	µF

8.0 MODULE FUNCTIONS

Parallel Interface

With the configured module chip, data transfers are done through an 8-bit bi-directional data bus (D7 to D0).

Moreover, data bus signals are recognized by a combination of A0, E, R/W signals, as shown in Table 9.

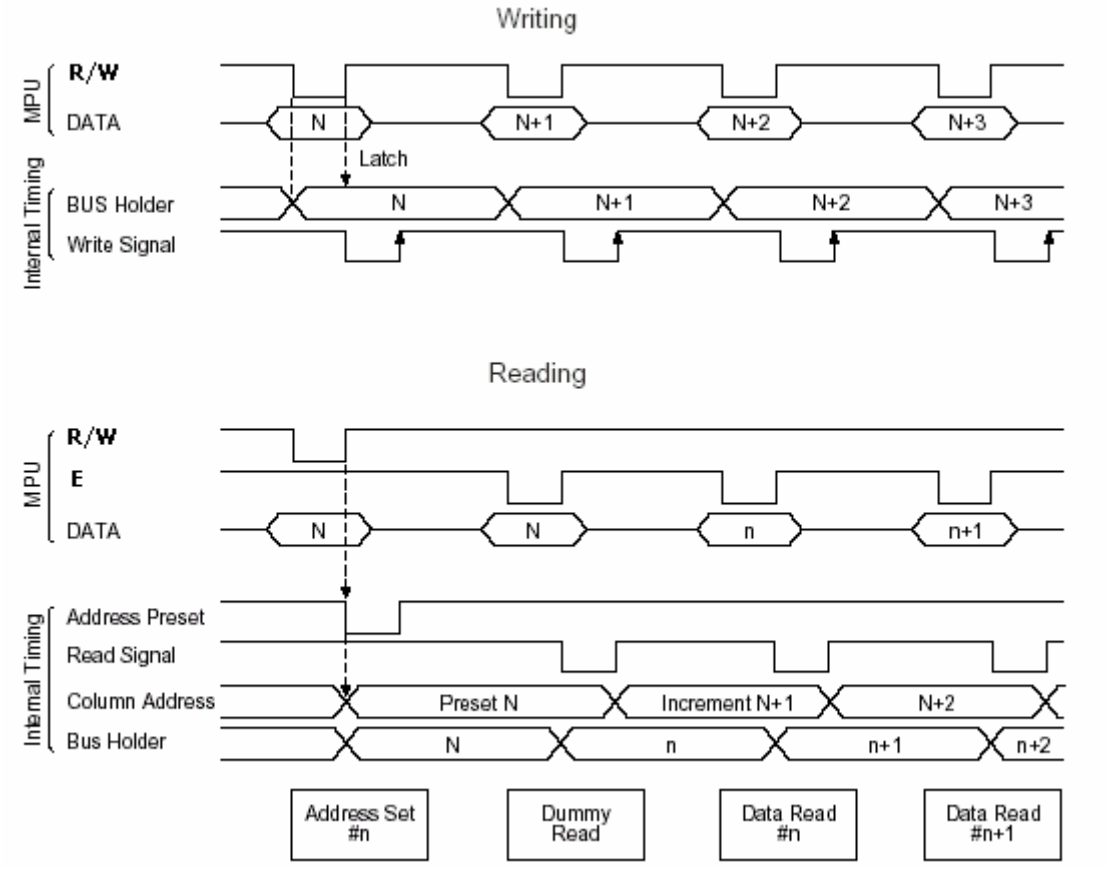
	6800 Series		Function
A0	R/W	E	
1	1	0	Reads the display data
1	0	1	Writes the display data
0	1	0	Status read
0	0	1	Write control data (command)

Accessing the Display Data RAM and the Internal Registers

Data transfer at a higher speed is ensured since the MPU is required to satisfy the cycle time (tCYC) requirement alone in accessing the module chip. Wait time may not be considered. And, in the module chip, each time data is sent from the MPU, a type of pipeline process between LSIs is performed through the bus holder attached to the internal data bus. For example, when the MPU writes data to the display data RAM, once the data is stored in the bus holder, then it is written to the display data RAM before the next data write cycle. Moreover, when the MPU reads the display data RAM, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle. There is a certain restriction in the read sequence of the display data RAM. Please be advised that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read of the second time. Thus, a dummy read is required whenever the address setup or write cycle operation is conducted. This relationship is shown in Figure 2.

The Busy Flag

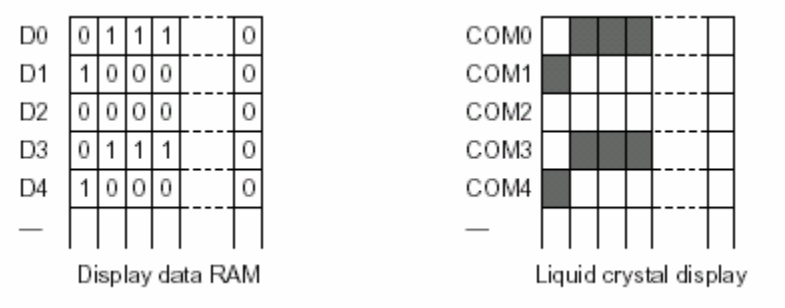
When the busy flag is "1" it indicates that the module chip is running internal processes, and at this time no command aside from a status read will be received. The busy flag is outputted to D7 pin with the read instruction. If the cycle time (tCYC) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.


Writing
MPU
R/W
DATA
N
N+1
N+2
N+3
Latch
Internal Timing
BUS Holder
Write Signal
N
N+1
N+2
N+3
Reading
MPU
R/W
E
DATA
N
N
n
n+1
Internal Timing
Address Preset
Read Signal
Column Address
Preset N
Increment N+1
N+2
Bus Holder
N
n
n+1
n+2
Address Set #n
Dummy Read
Data Read #n
Data Read #n+1

9.0 DISPLAY DATA RAM

Display Data RAM

The display data RAM is a RAM that stores the dot data for the display. It has a 65 (4 page X8 bit +1) X132 bit structure. It is possible to access the desired bit by specifying the page address and the column address. Because, as is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the liquid crystal display common direction. Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).



The Page Address Circuit

As shown in Figure 15, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.

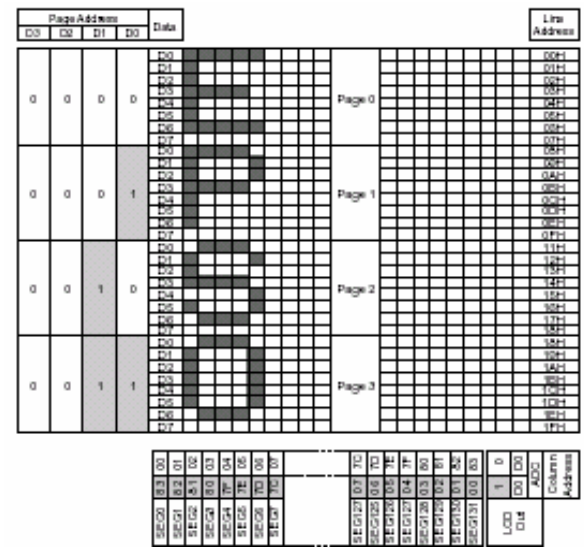
The Column Addresses

As is shown in Figure 15, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously. Moreover, the incrementation of column addresses stops with 83H but the display can only be seen column addresses with 78H 9(ADC"0") and only start to show display with column addresses 0CH with ADC "1" . Because the column address is independent of the page address, when moving, for example, from page 0 column 83H to page 1 column 00H, it is necessary to respecify both the page address and the column address. Furthermore, as is shown in Table 10, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. The Column addresses of the ADC select must carefully concern to avoid improper display pattern. (see approval drawing)

SEG Output	SEG0		SEG 131
ADC "0"	0 (H) →	Column Address	→ 83 (H)
(D0) "1"	83 (H) ←	Column Address	← 0 (H)

The Line Address Circuit

The line address circuit, as shown in Table 11, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified. (this is the COM0 output when the common output mode is normal, and the COM33 line area for the module chip . If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed.



The Common Output Status Select Circuit

In this module, the COM output scan direction can be selected by the common output status select command (See Table 11).

Status	COM Scan Direction
Normal	COM0 → COM31
Reverse	COM31 → COM0

10.0 LCD DISPLAY CONTROL

(1) Display ON/OFF

This command turns the display ON and OFF.

A0	E	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

When the display OFF command is executed when in the display all points ON mode, power saver mode is entered. See the section on the power saver for details.

(2) Display Start Line Set

This command is used to specify the display start line address of the display data RAM shown in Figure 18. For further details see the explanation of this function in "The Line Address Circuit".

A0	E	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
							↓				↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

(3) Page Address Set

This command specifies the page address corresponding to the low address when the MPU accesses the display data RAM (see Figure 18). Specifying the page address and column address enables to access a desired bit of the display data RAM. Changing the page address does not accompany a change in the status display.

A0	E	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
									↓		↓
							0	1	0	0	4

(4) Column Address Set

This command specifies the column address of the display data RAM shown in Figure 18. The column address is split into two sections (the higher 4 bits and the lower 4 bits) when it is set (fundamentally, set continuously). Each time the display data RAM is accessed, the column address automatically increments (+1), making it possible for the MPU to continuously read from/write to the display data. The column address increment is topped at 83H. This does not

change the page address continuously. See the function explanation in "The Column Address Circuit," for details.

	A0	E	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	Column address
HIGH bits →	0	1	0	0	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
LOW bits →							0	A3	A2	A1	A0	0	0	0	0	0	0	0	1	1
												0	0	0	0	0	0	1	0	2
	↓	↓																		
												1	0	0	0	0	0	1	0	130
												1	0	0	0	0	0	1	1	131

(5) Status Read

A0	E	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	When BUSY = 1, it indicates that either processing is occurring internally or a reset condition is in process. While the chip does not accept commands until BUSY = 0, if the cycle time can be satisfied, there is no need to check for BUSY conditions.
ADC	This shows the relationship between the column address and the segment driver. 0: Reverse (column address 131-n ↔ SEG n) 1: Normal (column address n ↔ SEG n) (The ADC command switches the polarity.)
ON/OFF	ON/OFF: indicates the display ON/OFF state. 0: Display ON 1: Display OFF (This display ON/OFF command switches the polarity.)
RESET	This indicates that the chip is in the process of initialization either because of a $\overline{RES}$ signal or because of a reset command. 0: Operating state 1: Reset in progress

(6) Display Data Write

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by "1" after the write, the MPU can write the display data.

A0	E	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

(7) Display Data Read

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by "1" after the read, the CPU can continuously read multiple-word data. One dummy read is required immediately after the column address has

been set. See the function explanation in "Display Data RAM" for the explanation of accessing the internal registers. When the serial interface is used, reading of the display data becomes unavailable.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

(8) ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output. Thus, sequence of the segment driver output pins may be reversed by the command. See the column address circuit (figure 18) for the detail. Increment of the column address (by "1") accompanying the reading or writing the display data is done according to the column address indicated in Figure 15.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

(9) Display Normal/Reverse

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM Data HIGH LCD ON voltage (normal)
										1	RAM Data LOW LCD ON voltage (reverse)

(10) Display All Points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the display data RAM. The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command. When the display is in an OFF mode, executing the display all points ON command will place the display in power save mode. For details, see the Power Save section.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all points ON

(11) LCD Bias Set

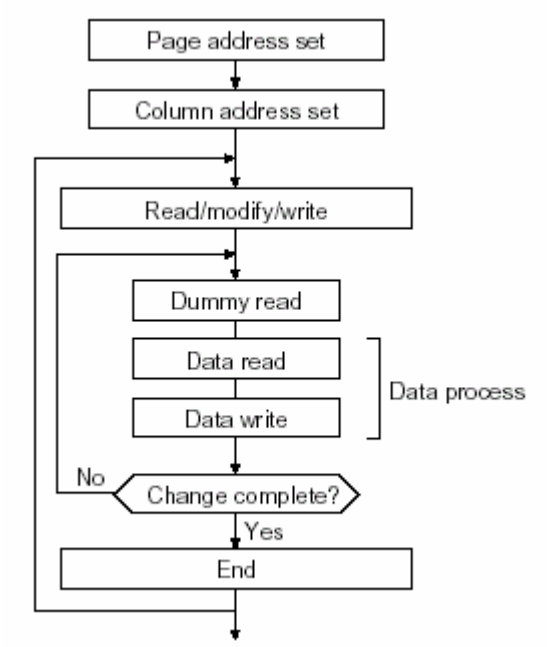
This command selects the voltage bias ratio required for the liquid crystal display. This command can be valid while the V/F circuit of Power Supply circuit is in operation.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Select Status
0	1	0	1	0	1	0	0	0	1	0	1/6 bias
										1	1/5 bias

(12) Read/Modify/Write

This command is used paired with the "END" command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments (+1) the column address. This mode is maintained until the END command is input. When the END command is input, the column address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.
*** Even in read/modify/write mode, other commands aside from display data read/write commands can also be used. However, the column address set command cannot be used.**

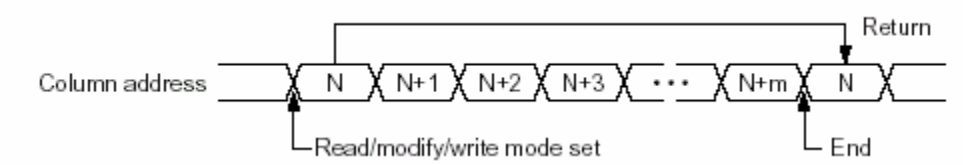
A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0



(13) End

This command releases the read/modify/write mode, and returns the column address to the address it was at when the mode was entered.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



(14) Reset

This command initializes the display start line, the column address, the page address, the common output mode, the V5 voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and the read/modify/ write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in "Reset" for details. The reset operation is performed after the reset command is entered. The initialization when the power supply is applied must be done through applying a reset signal to the RES terminal. The reset command must not be used instead.

A0	E	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

(15) Common Output Mode Select

This command can select the scan direction of the COM output terminal. For details, see the function explanation in "Common Output Mode Select Circuit."

A0	E	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	1	1	0	0	0	*	*	*	COM0→COM31
							1				COM31→COM0

(16) Power Controller Set

This command sets the power supply circuit functions. See the function explanation in "The Power Supply Circuit," for details

A0	E	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	0	0	1	0	1	0			Booster circuit: OFF
								1			Booster circuit: ON
									0		Voltage regulator circuit: OFF
									1		Voltage regulator circuit: ON
										0	Voltage follower circuit: OFF
										1	Voltage follower circuit: ON

(17) V5 Voltage Regulator Internal Resistor Ratio Set

This command sets the V5 voltage regulator internal resistor ratio. For details, see the function explanation is "The Power Supply Circuits."

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									↓		↓
								1	1	0	
								1	1	1	Large

(18) The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal drive voltage V5 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

• The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

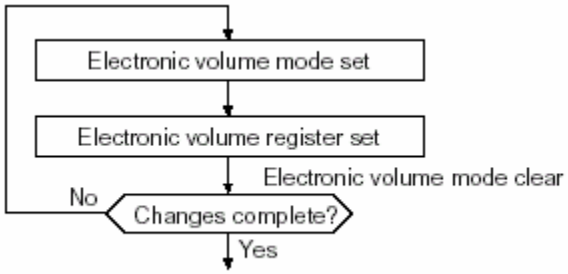
• Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V5 assumes one of the 64 voltage levels. When this command is input, the electronic volume mode is released after the electronic volume register has been set. When the electronic volume function is not used, set this to (1, 0, 0, 0, 0, 0)

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	| V5 |
0	1	0	*	*	0	0	0	0	0	1	Small
0	1	0	*	*	0	0	0	0	1	0	
0	1	0	*	*	0	0	0	0	1	1	
						↓					↓
0	1	0	*	*	1	1	1	1	1	0	
0	1	0	*	*	1	1	1	1	1	1	Large

* Inactive bit

• The Electronic Volume Register Set Sequence
Figure 26



(19) Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands. This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes. The static indicator ON command is a double byte command paired with the static indicator register set command, and thus one must execute one after the other. (The static indicator OFF command is a single byte command.)

• Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	E	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Static Indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

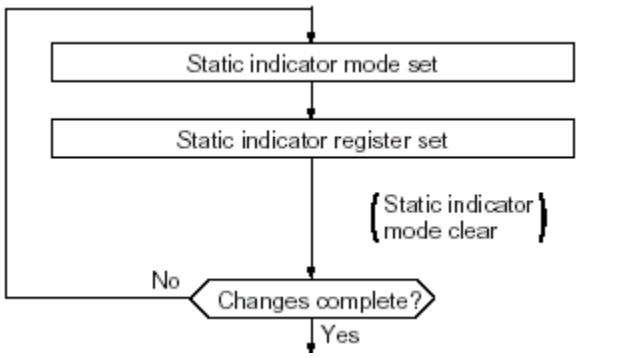
• Static Indicator Register Set

This command sets two bits of data into the static indicator register, and is used to set the static indicator into a blinking mode.

A0	E	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Indicator Display State
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinking at approximately one second intervals)
									1	0	ON (blinking at approximately 0.5 second intervals)
									1	1	ON (constantly on)

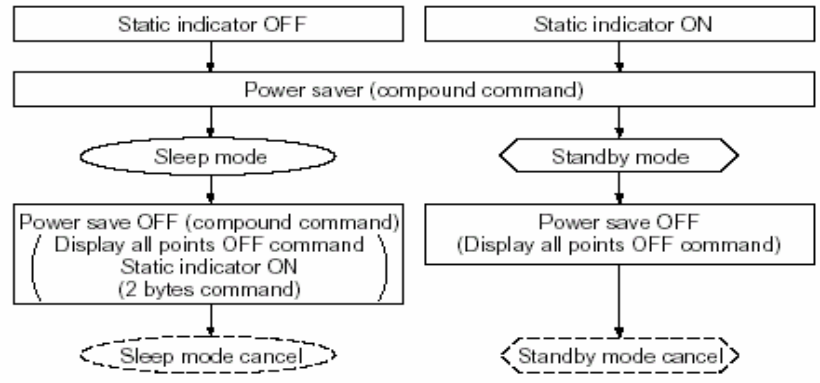
* Disabled bit

• Static Indicator Register Set Sequence
Figure 17



(20) Power Save (Compound Command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered, thus greatly reducing power consumption. The power saver mode has two different modes: the sleep mode and the standby mode. When the static indicator is OFF, it is the sleep mode that is entered. When the static indicator is ON, it is the standby mode that is entered. In the sleep mode and in the standby mode, the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM. Refer to figure 28 for power save off sequence.
Figure 22



• Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:
1 The oscillator circuit and the LCD power supply circuit are halted.
2 All liquid crystal drive circuits are halted, and the segment in common drive outputs output a VDD level.

• Standby Mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive. The internal modes are in the following states during standby mode.
1 The LCD power supply circuits are halted. The oscillator circuit continues to operate.

2 The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs output a VDD level. The static drive system does not operate.
When a reset command is performed while in standby mode, the system enters sleep mode.
*** When an external power supply is used, it is recommended that the functions of the external power supply circuit be stopped when the power saver mode is started. For example, when the various levels of liquid crystal drive voltage are provided by external resistive voltage dividers, it is recommended that a circuit be added in order to cut the electrical current flowing through the resistive voltage divider circuit when the power saver mode is in effect. The S1D15605 series chips have a liquid crystal display blanking control terminal DOF. This terminal enters an LOW state when the power saver mode is launched. Using the output of DOF, it is possible to stop the function of an external power supply circuit.**
*** When the master is turned on, the oscillator circuit is operable immediately after the powering on.**

(21) NOP

Non-Operation Command

A0	E	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

11. COMMAND SAMPLE SEQUENCE

	Command	Command Code A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0/1	LCD display ON/OFF 0: OFF, 1: ON
(2)	Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3)	Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4)	Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address
	Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address
(5)	Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6)	Display data write	1	1	0	Write data								Writes to the display RAM
(7)	Display data read	1	0	1	Read data								Reads from the display RAM
(8)	ADC select	0	1	0	1	0	1	0	0	0	0	0/1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9)	Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0/1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10)	Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Display all points 0: normal display 1: all points ON
(11)	LCD bias set	0	1	0	1	0	1	0	0	0	1	0/1	0: 1/6, 1: 1/5
(12)	Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13)	End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14)	Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15)	Common output mode select	0	1	0	1	1	0	0	0/1	*	*	*	Select COM output scan direction 0: normal direction, 1: reverse direction
(16)	Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17)	V0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio (Rb/Ra) mode
(18)	Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	
	Electronic volume register set	0	1	0	*	*	Electronic volume value						Set the V0 output voltage electronic volume register
(19)	Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0/1	0: OFF, 1: ON
	Static indicator register set	0	1	0	*	*	*	*	*	*	Mode		Set the flashing mode
(20)	Power saver												Display OFF and display all points ON compound command
(21)	NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22)	Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

(Note) *: disabled data

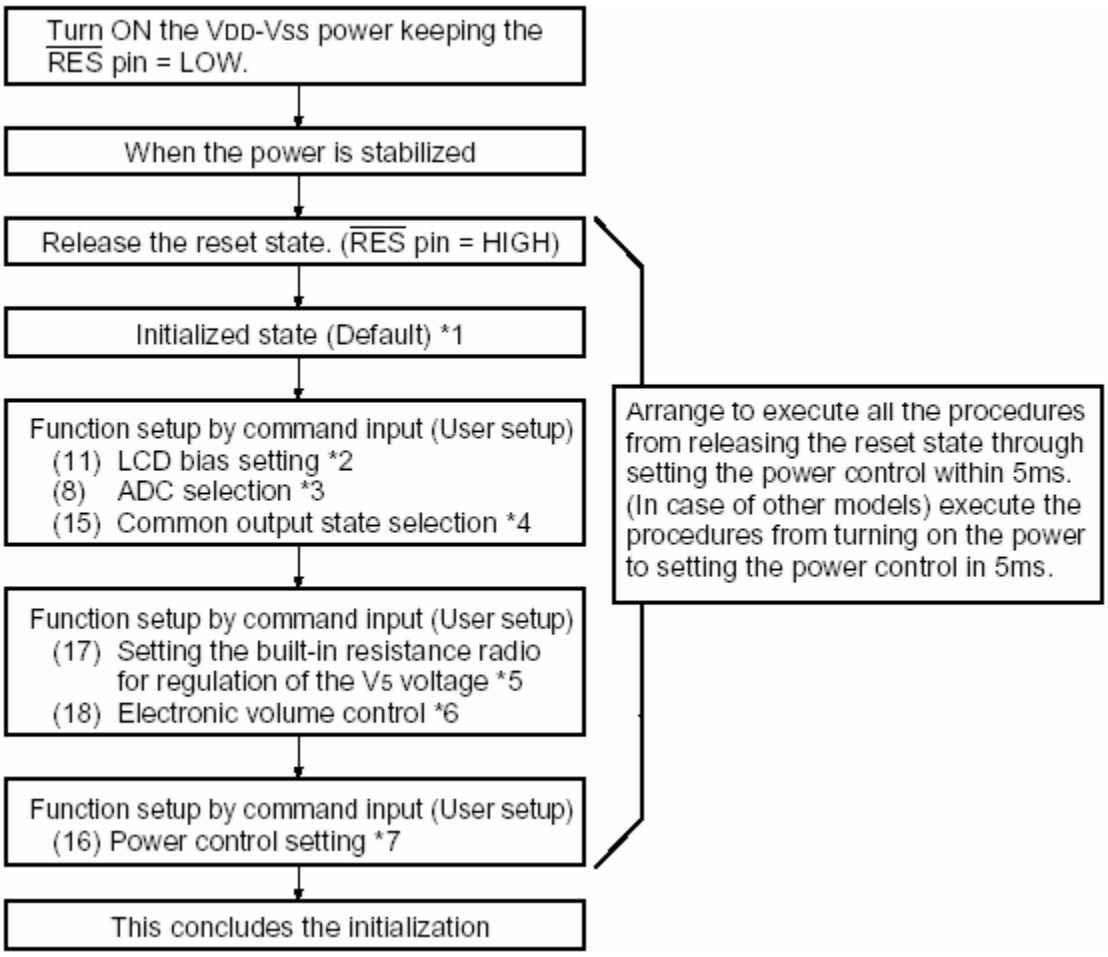
12.0 COMMAND DESCRIPTION

Instruction Setup: Reference (reference)

Initialization:

Note: With this IC, when the power is applied, LCD driving non-selective potentials V2 and V3 (SEG pin) and V1 and V4 (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins (V1 ~ V5) and the VDD pin, the picture on the display may become totally dark instantaneously when the power is turned on. To avoid occurrence of such a failure, we recommend the following flow when turning on the power.

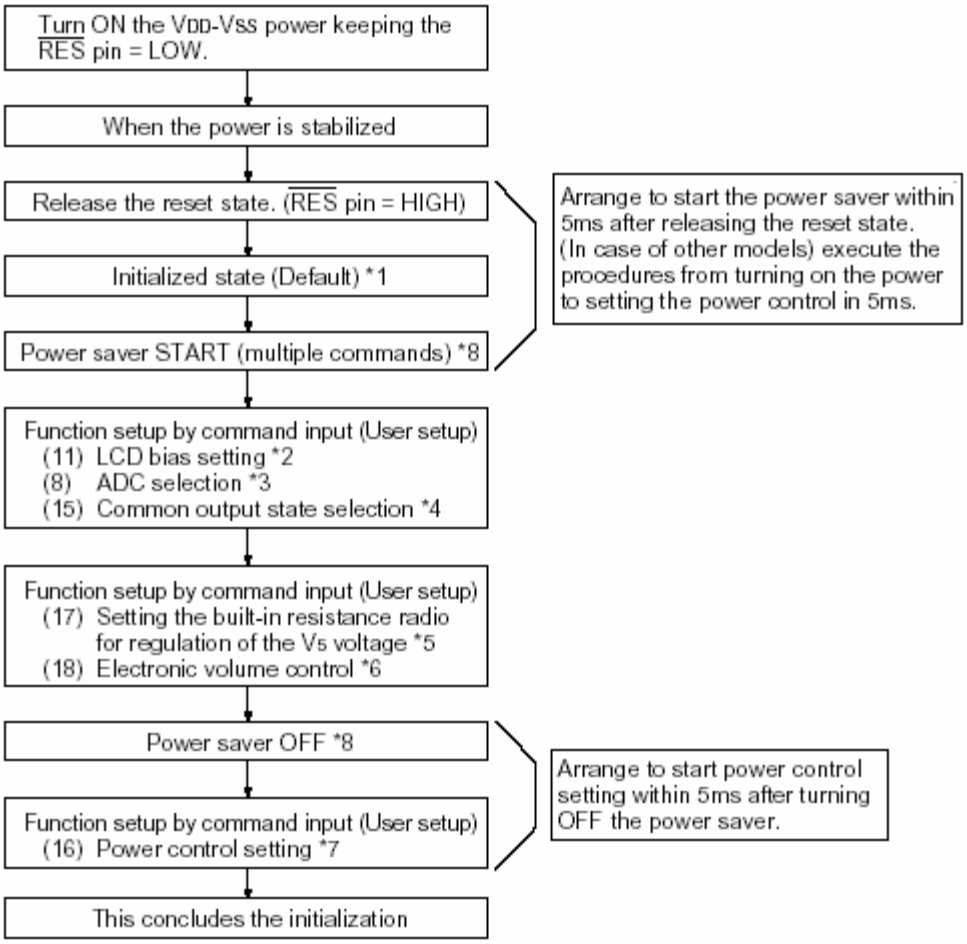
1. When the built-in power is being used immediately after turning on the power:



*** The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.**

Notes: Refer to respective sections or paragraphs listed below.
***1: 6. Description of functions; "Resetting circuit" (If takes not more than 2 ms from Power Supply ON to the stability of internal oscillating circuit.)**
***2: 7. Command description; "(11) LCD bias setting"**
***3: 7. Command description; "(8) ADC selection"**
***4: 7. Command description; "(15) Common output state selection"**
***5: 6. Description of functions; "Power circuit" & Command description; "(17) Setting the built-in resistance radio for regulation of the V5 voltage"**
***6: 6. Description of functions; "Power circuit" & Command description; "(18) Electronic volume control"**
***7: 6. Description of functions; "Power circuit" & Command description; "(16) Power control setting"**

2. When the built-in power is not being used immediately after turning on the power:

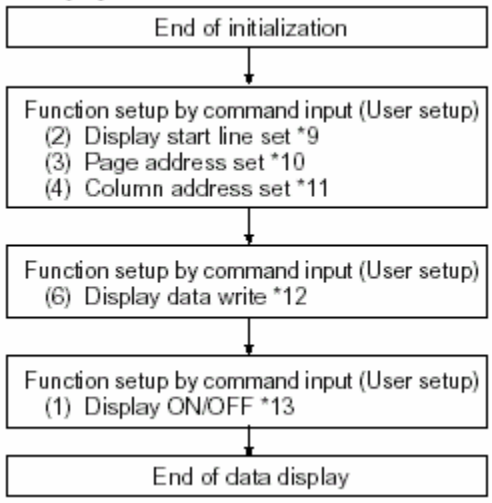


*** The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.**

Notes: Refer to respective sections or paragraphs listed below.
***1: 6. Description of functions; "Resetting circuit" (The contents of DDRAM can be variable even in the**
initial setting (Default) at the reset state.)

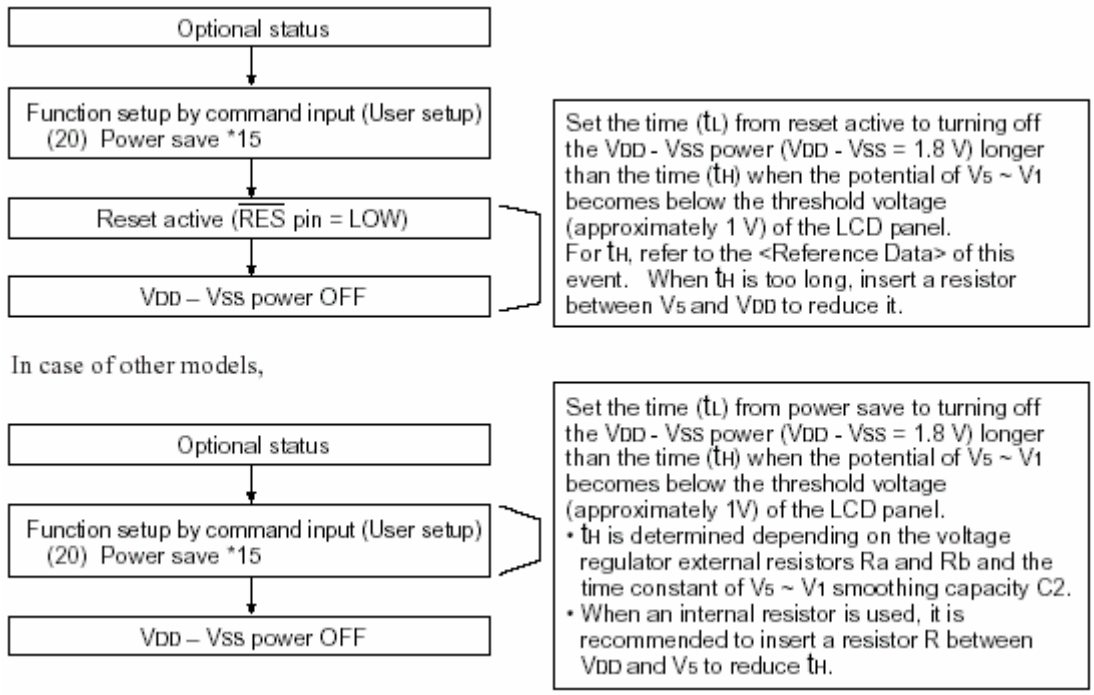
***2: 7. Command description; "(11) LCD bias setting"**
***3: 7. Command description; "(8) ADC selection"**
***4: 7. Command description; "(15) Common output state selection"**
***5: 6. Description of functions; "Power circuit" & "(17) Command description; Setting the built-in**
resistance radio for regulation of the V5 voltage"
***6: 6. Description of functions; "Power circuit" & "(18) Command description; Electronic volume control"**
***7: 6. Description of functions; "Power circuit" & "(16) Command description; Power control setting"**
***8: 7. The power saver ON state can either be in sleep state or stand-by state.**
Command description; "Power saver START (multiple commands)"

Data Display



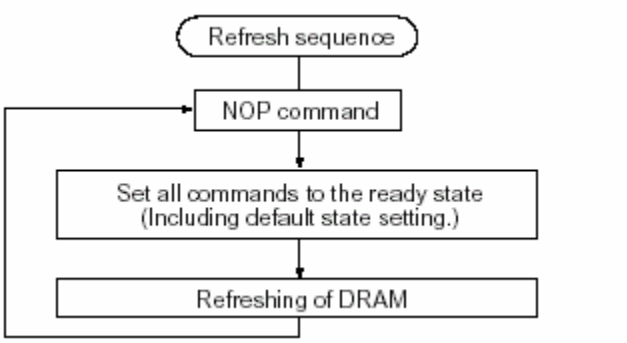
Notes: Reference items
*9: Command Description; Display start line set
*10: Command Description; Page address set
*11: Command Description; Column address set
*12: Command Description; Display data write
*13: Command Description; Display ON/OFF
Avoid displaying all the data at the data display start (when the display is ON) in white.

Power OFF *14



***14: The logic circuit of this IC's power supply VDD - VSS controls the driver of the LCD power supply VDD - V5. So, if the power supply VDD - VSS is cut off when the LCD power supply VDD - V5 has still any residual voltage, the driver (COM. SEG) may output any uncontrolled voltage. When turning off the power, observe the following basic procedures:**
• After turning off the internal power supply, make sure that the potential V5 ~ V1 has become below the threshold voltage of the LCD panel, and then turn off this IC's power supply (VDD - VSS).
6. Description of Function, 6.7 Power Circuit
***15: After inputting the power save command, be sure to reset the function using the RES terminal until the**
power supply VDD - VSS is turned off. 7. Command Description (20) Power Save
***16: After inputting the power save command, do not reset the function using the RES terminal until the**
power supply VDD - VSS is turned off. 7. Command Description (20) Power Save

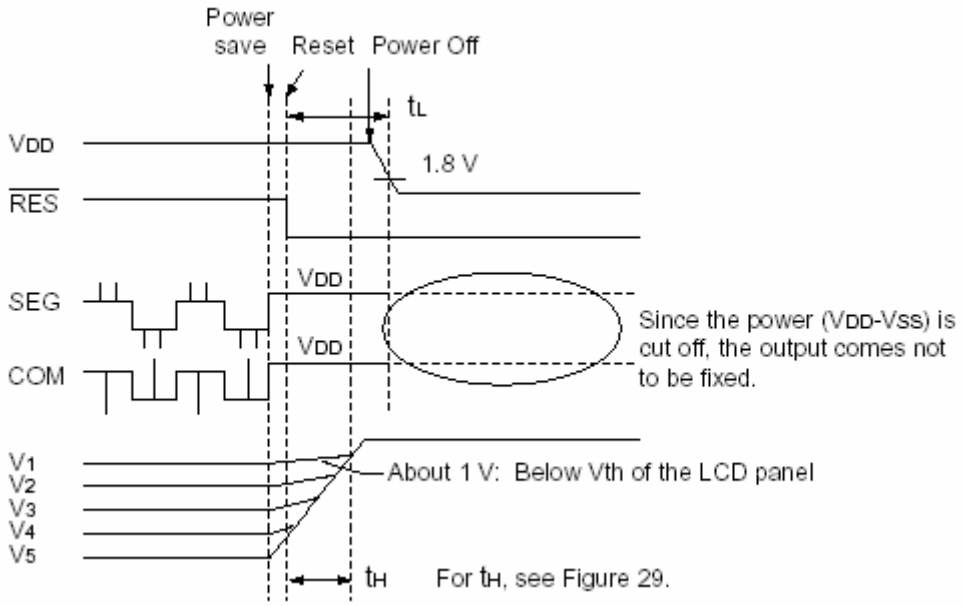
Refresh



It is recommended that the operating modes and display contents be refreshed periodically to prevent the effect of unexpected noise

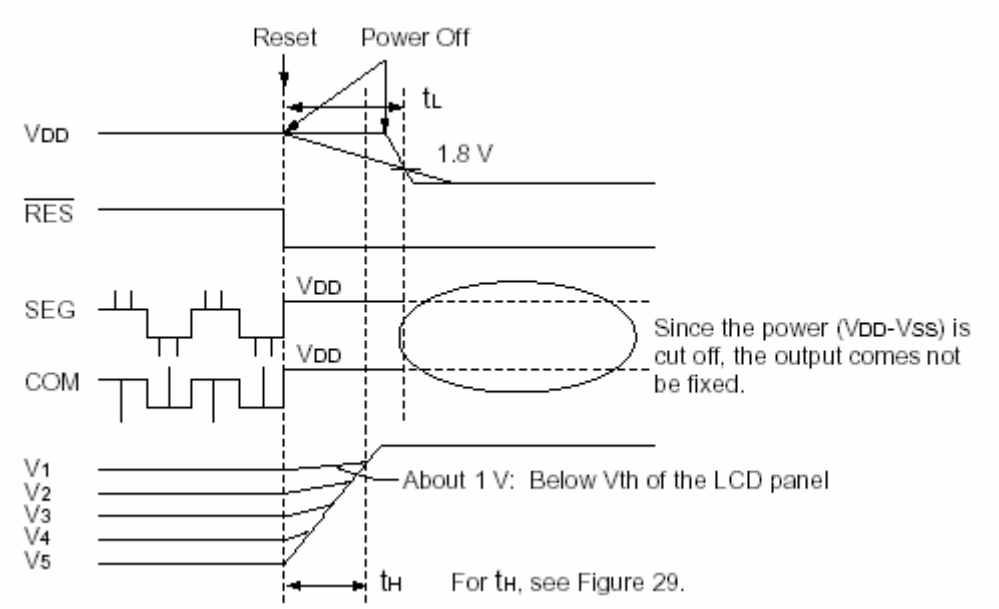
Precautions on Turning off the power

Observe Paragraph 1) as the basic rule.
<Turning the power (VDD - VSS) off>
1) Power Save (The LCD powers (VDD - V5) are off.) →rearrange input →Power (VDD - VSS) OFF
• Observe tL > tH.
• When tL < tH, an irregular display may occur.
Set tL on the MPU according to the software. tH is determined according to the external capacity C2 (smoothing capacity of V5 ~ V1) and the driver's discharging capacity.

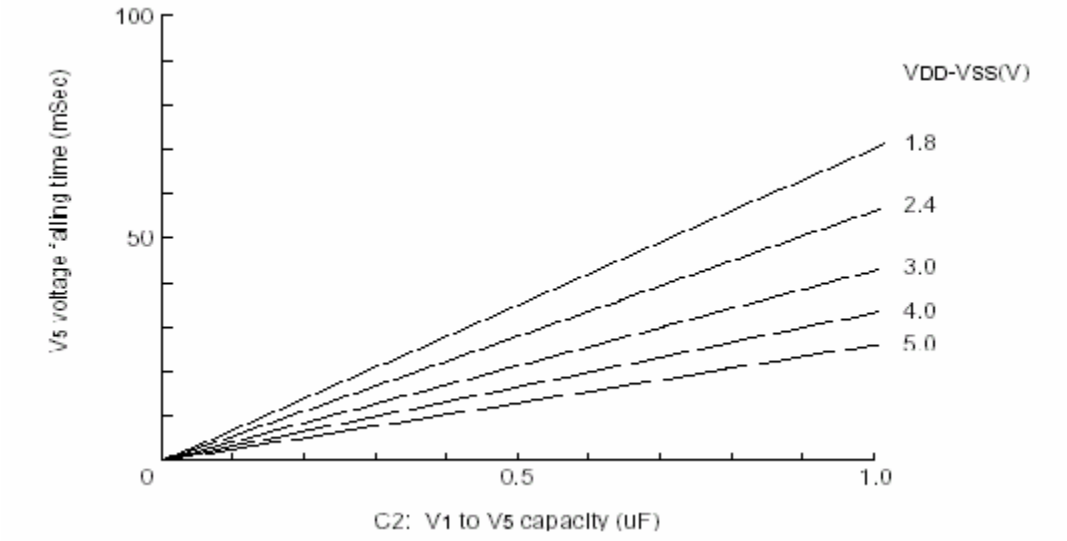


<Turning the power (VDD - VSS) off : When command control is not possible.>
2) Reset (The LCD powers (VDD - VSS) are off.) →Power (VDD - VSS) OFF

• Observe tL > tH.
• When tL < tH, an irregular display may occur.
For tL, make the power (VDD - VSS) falling characteristics longer or consider any other method. tH is determined according to the external capacity C2 (smoothing capacity of V5 to V1) and the driver's discharging capacity.

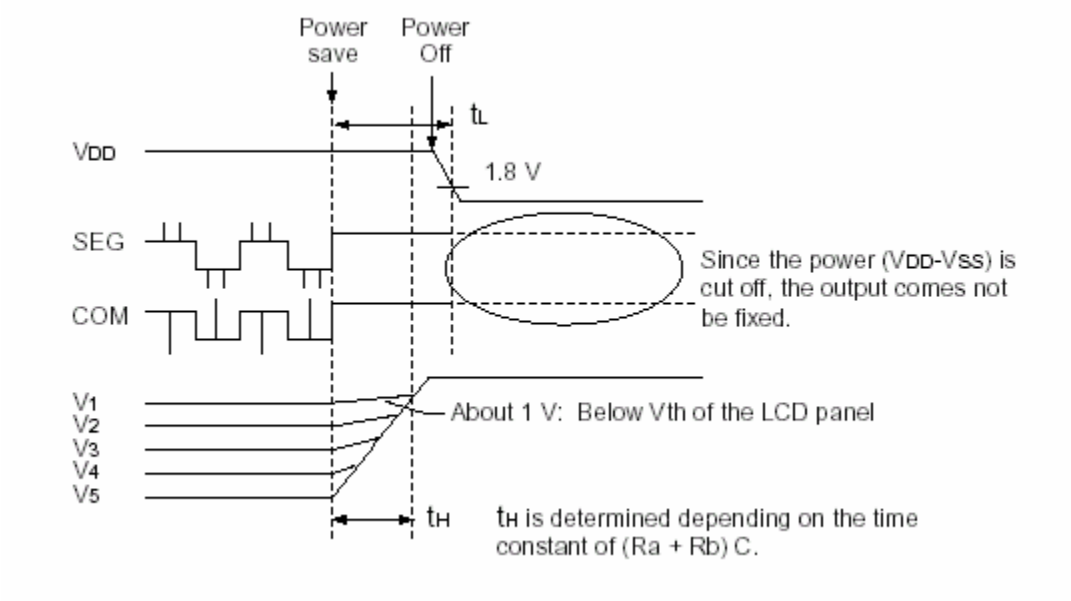


<Reference Data>
V5 voltage falling (discharge) time (tH) after the process of operation → power save → reset.
V5 voltage falling (discharge) time (tH) after the process of operation → reset.



• In case of other models than the above
<Turning the power (VDD - VSS) off>
Power save (The LCD powers (VDD - VSS) are off.) -> Power (VDD - VSS) OFF
• Observe tL > tH.
• When tL < tH, an irregular display may occur.

Set tL on the MPU according to the software. tH is determined according to the external capacity C (smoothing capacity of V5 to V1) and the external resisters Ra + Rb (for V5 voltage regulation)



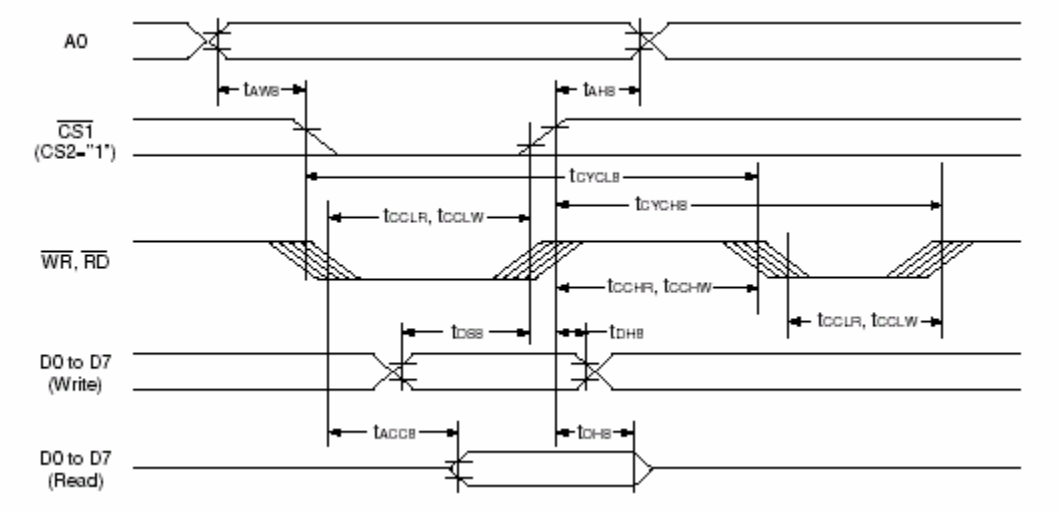
13.0 ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Supply voltage range	VDD	-0.3 to 7.0	V
Operating temperature Range	T_{OPR}	-20 to +70	°C
Storage temperature Range	T_{STG}	-30 to +80	°C

14.0 DC Module ELECTRICAL CHARACTERISTICS

No	Item	Symbol	Condition	Min	Typ	Max	Unit
1.	Operating voltage	V_{DD}	-	2.7	3.0	3.6	V
2.	Power Supply Current	I_{OP}	-	-	500	900	uA
3.	LCD Driving Voltage	V_{LCD}	V5 - V_{DD}	-	9.0±5%	-	V

15.0 SYSTEM BUS READ/WRITE CHARACTERISTICS (8080)



(V_{DD} = 2.7 V to 3.6 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time 1	A0	t_{CYCL8}		300	—	ns
System cycle time 2		t_{CYCH8}		300	—	ns
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		60	—	ns
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		120	—	ns
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		60	—	ns
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		60	—	ns
Data setup time	D0 to D7	t_{DS8}		40	—	ns
Data hold time		t_{DH8}		15	—	ns
$\overline{RD}$ access time		t_{ACC8}	CL = 100 pF	—	140	ns
Output disable time		t_{OH8}		10	100	ns

(V_{DD} = 2.4 V to 3.0 V, Ta = –40 to 85°C)

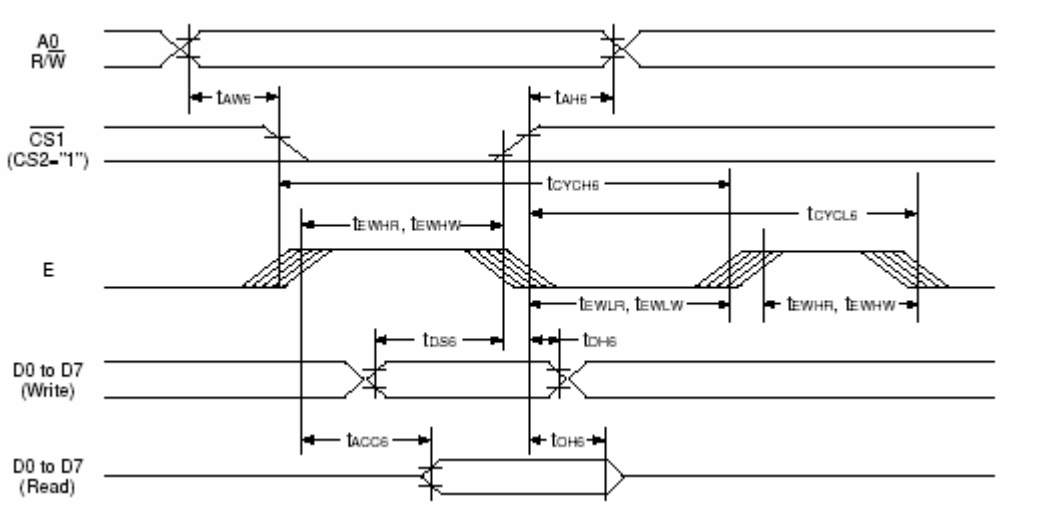
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time 1	A0	t_{CYCL8}		450	—	ns
System cycle time 2		t_{CYCH8}		450	—	ns
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		90	—	ns
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		180	—	ns
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		90	—	ns
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		90	—	ns
Data setup time	D0 to D7	t_{DS8}		60	—	ns
Data hold time		t_{DH8}		20	—	ns
$\overline{RD}$ access time		t_{ACC8}	CL = 100 pF	—	230	ns
Output disable time		t_{OH8}		10	150	ns

(V_{DD} = 1.8 V to 2.4 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time 1	A0	t_{CYCL8}		600	—	ns
System cycle time 2		t_{CYCH8}		600	—	ns
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		120	—	ns
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		240	—	ns
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		120	—	ns
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		120	—	ns
Data setup time	D0 to D7	t_{DS8}		80	—	ns
Data hold time		t_{DH8}		30	—	ns
$\overline{RD}$ access time		t_{ACC8}	CL = 100 pF	—	280	ns
Output disable time		t_{OH8}		10	200	ns

***1 This is in the case of making the access by WR and RD,setting the CS1=LOW.**
***2 This is the case of making the accese by CS1,setting the WR,RD=LOW.**
***3 The rise and fall times (tr and tf) of the input signal are specified for less than 15 ns.When using the**
system cycle time at high speed, they are specified for (tr + tf) (tCYC8-tCCLR-tCCHR).
***4 All timings are specified based on the 20 and 80% of VDD.**
***5 tCCLW and tCCLR are specified for the overlap period when CS1 is at LOW (CS2=HIGH) level and**

15.1 SYSTEM BUS READ/WRITE CHARACTERISTICS (68000)



(V_{DD} = 2.7 V to 3.6 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating Min.	Rating Max.	Units
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns ns
System cycle time 1 System cycle time 2		A0	t_{CYCH6} t_{CYCL6}		300 300	— —	ns ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		40 15	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	CL = 100 pF	— 10	140 100	ns ns
Enable HIGH pulse time	Read Write	E	t_{EWHR} t_{EWHW}		120 60	— —	ns ns
Enable LOW pulse time	Read Write	E	t_{EWLR} t_{EWLW}		60 60	— —	ns ns

(V_{DD} = 2.4 V to 3.0 V, Ta = –40 to 85°C)

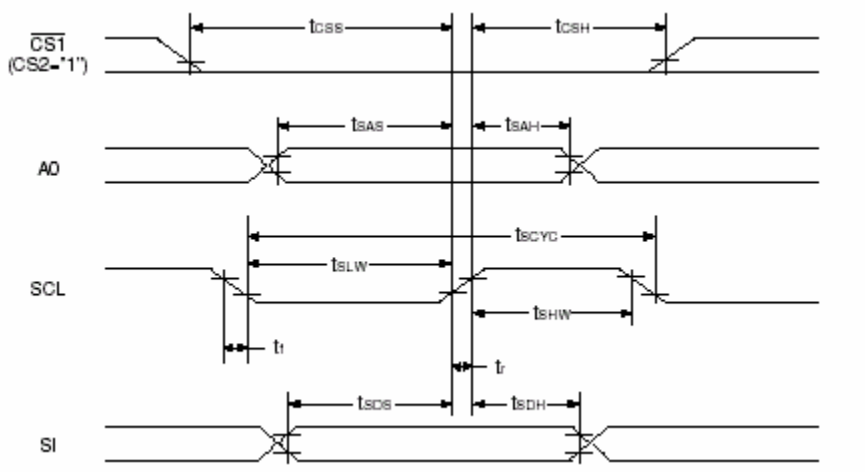
Item		Signal	Symbol	Condition	Rating Min.	Rating Max.	Units
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns ns
System cycle time 1 System cycle time 2		A0	t_{CYCH6} t_{CYCL6}		450 450	— —	ns ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		60 20	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	CL = 100 pF	— 10	230 150	ns ns
Enable HIGH pulse time	Read Write	E	t_{EWHR} t_{EWHW}		180 90	— —	ns ns
Enable LOW pulse time	Read Write	E	t_{EWLR} t_{EWLW}		90 90	— —	ns ns

(V_{DD} = 1.8 V to 2.4 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns ns
System cycle time 1 System cycle time 2		A0	t_{CYCH6} t_{CYCL6}		600 600	— —	ns ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		80 30	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	CL = 100 pF	— 10	280 200	ns ns
Enable HIGH pulse time	Read Write	E	t_{EWHR} t_{EWHW}		240 120	— —	ns ns
Enable LOW pulse time	Read Write	E	t_{EWLR} t_{EWLW}		120 120	— —	ns ns

***1 This is in the case of making the access by E, setting the CS1=LOW.**
***2 This is the case of making the access by CS1,setting the E=HIGH.**
***3 The rise and fall times ((tr and tf) of the input signal are specified for less than 15 ns.When using the**
system cycle time at high speed, they are specified for (tr + tf) (tCYC6-tEWLW-tEWHW) or (tr + tf)
(tCYC6-tEWLR-tEWHR).
***4 All timings are specified based on the 20 and 80% of VDD.**
***5 tEWLW and tEWLR are specified for the overlap period when CS1 is at LOW (CS2=HIGH) level and E**
is at the HIGH level.

15.2 SERIAL INTERFACE



(VDD = 2.7 V to 3.6 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		250	—	ns
SCL HIGH pulse width		tSHW		100	—	ns
SCL LOW pulse width		tSLW		100	—	ns
Address setup time	A0	tSAS		150	—	ns
Address hold time		tSAH		150	—	ns
Data setup time	SI	tSDS		100	—	ns
Data hold time		tSDH		100	—	ns
CS-SCL time	CS	tCSS		150	—	ns
		tCSH		150	—	ns

(VDD = 2.4 V to 3.0 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		300	—	ns
SCL HIGH pulse width		tSHW		125	—	ns
SCL LOW pulse width		tSLW		125	—	ns
Address setup time	A0	tSAS		200	—	ns
Address hold time		tSAH		200	—	ns
Data setup time	SI	tSDS		125	—	ns
Data hold time		tSDH		125	—	ns
CS-SCL time	CS	tCSS		200	—	ns
		tCSH		200	—	ns

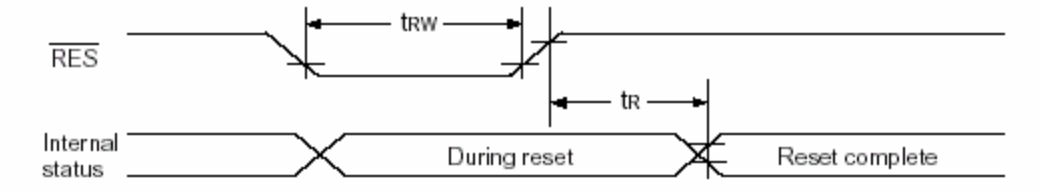
Table 44

(V_{DD} = 1.8 V to 2.4 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		400	—	ns
SCL HIGH pulse width		t_{SHW}		150	—	ns
SCL LOW pulse width		t_{SLW}		150	—	ns
Address setup time	A0	t_{SAS}		250	—	ns
Address hold time		t_{SAH}		250	—	ns
Data setup time	SI	t_{SDS}		150	—	ns
Data hold time		t_{SDH}		150	—	ns
CS-SCL time	CS	t_{CSS}		250	—	ns
		t_{CSH}		250	—	ns

***1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.**
***2 All timing is specified using 20% and 80% of VDD as the standard.**

Reset Input Timing



(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

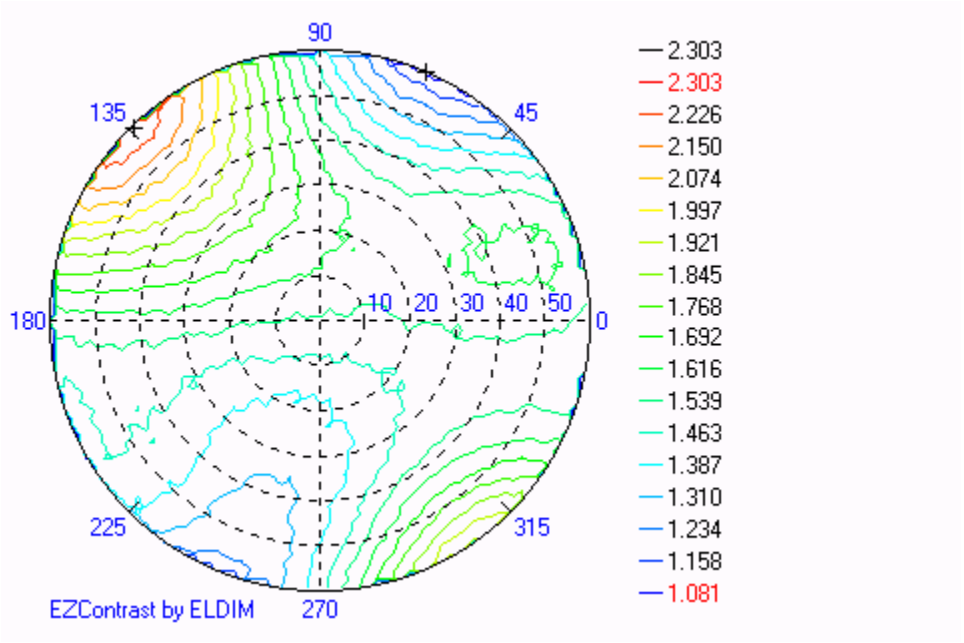
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1	µs
Reset LOW pulse width	RES	t_{RW}		1	—	—	µs

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1.5	µs
Reset LOW pulse width	RES	t_{RW}		1.5	—	—	µs

16.0 Optical Characteristics

1) LUMINANCE ON STATE

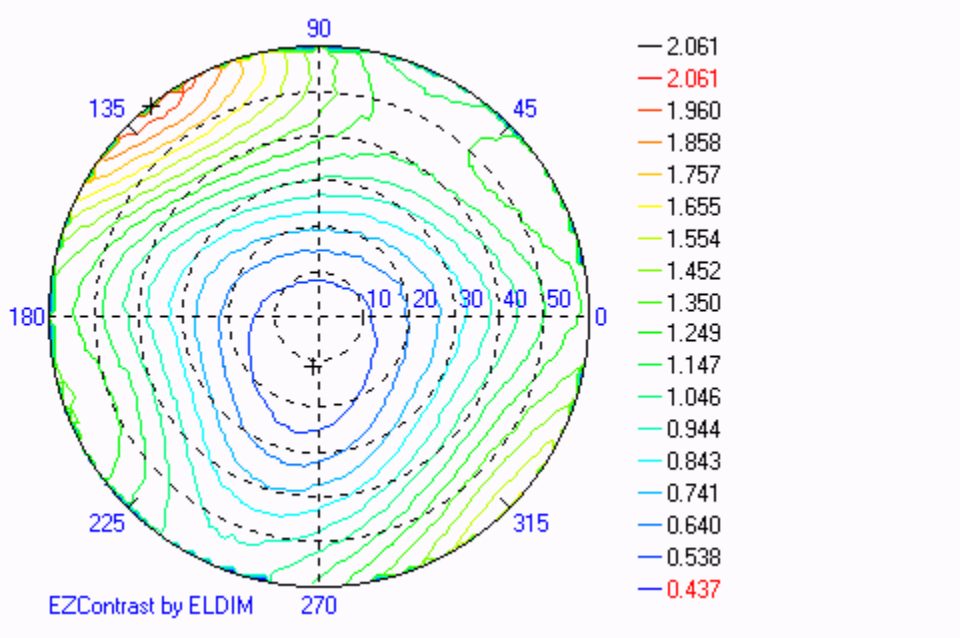


Measurement Condition:
a) Room Temperature
b)Static properties
c) Frequency = 64Hz

Measure Result:

Luminance Max = 2.303cd/m2

2) LUMINANCE OFF STATE

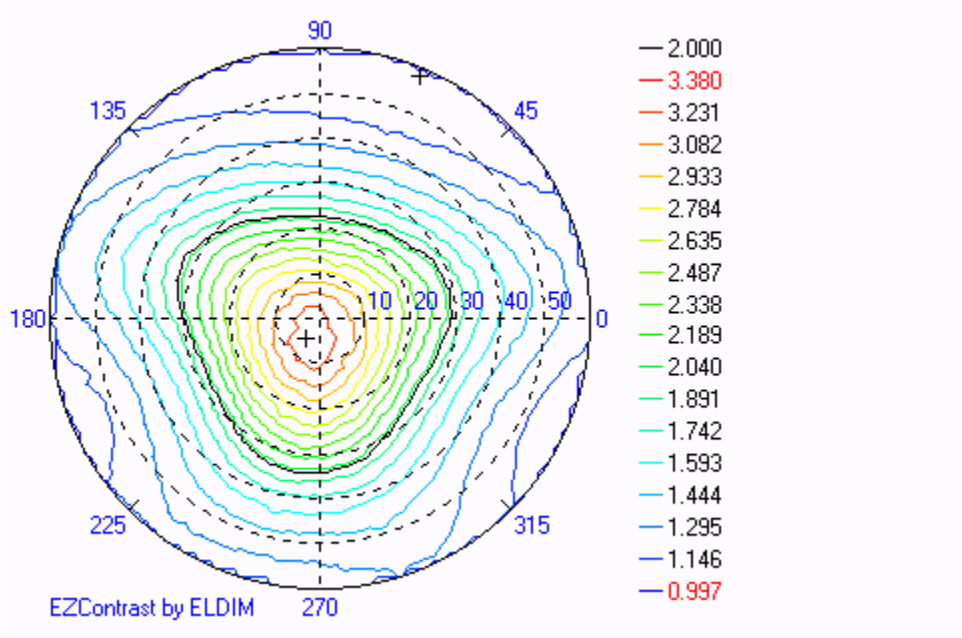


Measurement Condition:
a) Room Temperature
b)Multiplex properties
c) Frequency = 64Hz

Measure Result:

Luminance Max = 2.061cd/m2

3) CONTRAST RATIO (A NUMBER OF PIXELS)

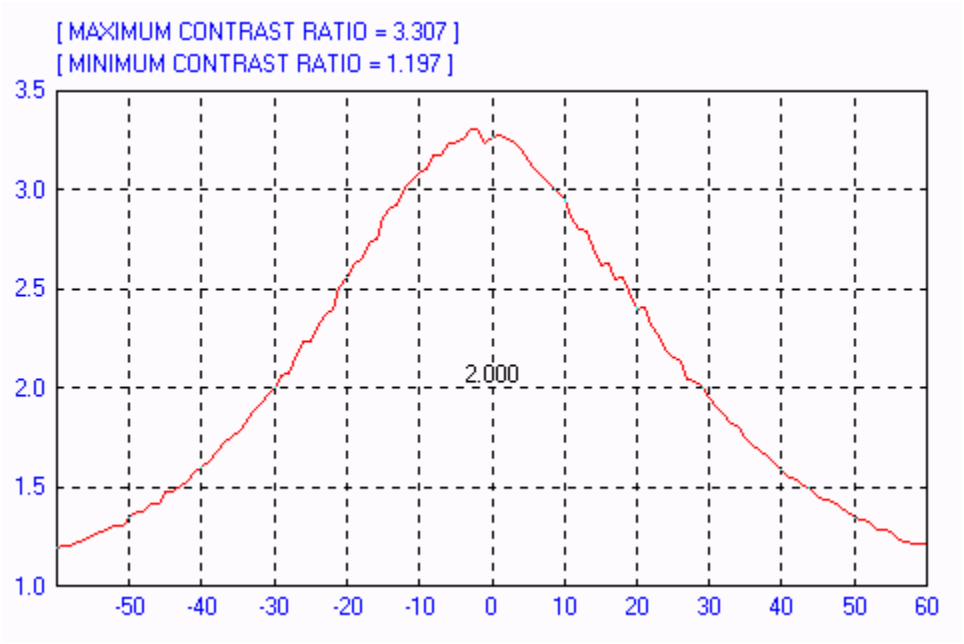


Measurement Condition:
a) Room Temperature
b)Multiplex properties
c) Frequency = 64Hz

Measure Result:

Contrast Ratio at Head on (θ = 0) =3.2

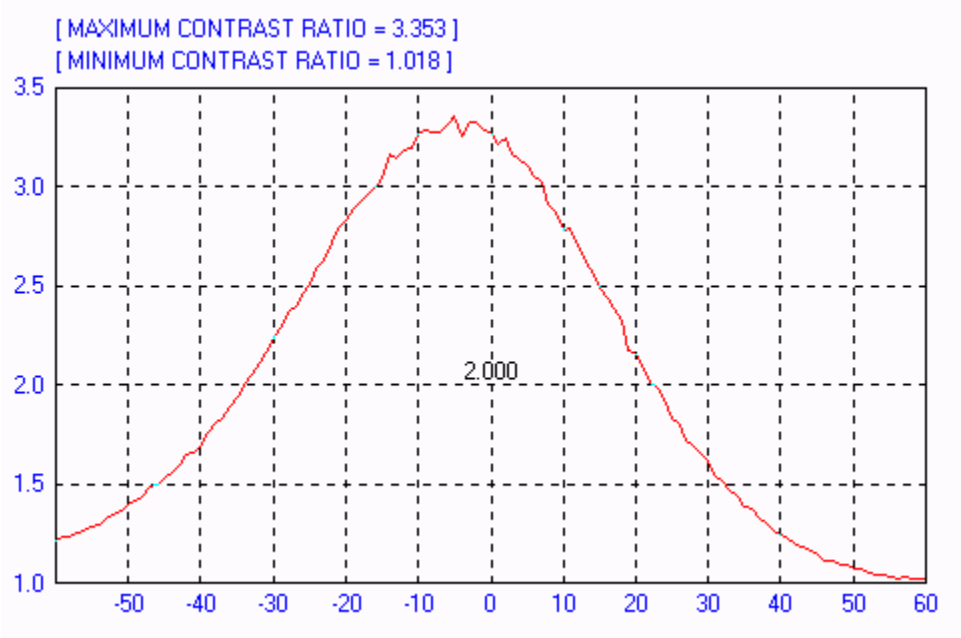
4). CONTRAST RATIO AT HORIZONTAL(A NUMBER OF PIXELS)



Measurement Condition:
a) Room Temperature
b)Multiplex properties
c) Frequency = 64Hz

Measure Result:

Contrast Ratio >=2 =-30°+28°



Measurement Condition:
a) Room Temperature
b)Multiplex properties
c) Frequency = 64Hz

Measure Result:

Contrast Ratio >=2 =-34°+22°

6. RESPONSE TIME

Ton =241.18ms
Toff =170.59ms

Measurement Condition:
a) Room Temperature
b)Multiplex properties
c) Frequency = 64Hz

17.0 SAMPLE PROGRAMMING

MPU = PIC16C74A
INITIALIZATION ROUTINE

```
                     00149 ; SETTING S1D15607D00B
                     00150 ; S1D15607D00b INIT
                     00151
0035   30E2          00152                MOVLW   0XE2
0036   00A2          00153                MOVWF   CMDO
0037   21BC          00154                CALL    SEND_C
                     00155
0038   21C6          00156                CALL    DELAY
                     00157
0039   30A3          00158                MOVLW   0XA3            ;BIAS 1/9
003A   00A2          00159                MOVWF   CMDO
003B   21BC          00160                CALL    SEND_C
                     00161
003C   30A0          00162                MOVLW   0XA0            ;ADC S1 -S132
003D   00A2          00163                MOVWF   CMDO
003E   21BC          00164                CALL    SEND_C
                     00165
003F   30C0          00166                MOVLW   0XC0            ;SHL COM1 -COM64   C0
0040   00A2          00167                MOVWF   CMDO
0041   21BC          00168                CALL    SEND_C
                     00169
0042   3025          00170                MOVLW   0X25            ;REGULATOR SELECT
0043   00A2          00171                MOVWF   CMDO
0044   21BC          00172                CALL    SEND_C
                     00173
0045   21C6          00174                CALL    DELAY
0046   21C6          00175                CALL    DELAY
                     00176
0047   3081          00177                MOVLW   0X81            ;REFERENCE VOLTAGE SELECT
0048   00A2          00178                MOVWF   CMDO
0049   21BC          00179                CALL    SEND_C
                     00180
004A   21C6          00181                CALL    DELAY
004B   21C6          00182                CALL    DELAY
                     00183
004C   302C          00184                MOVLW   0X2C            ;COEFFICIENT 2D
004D   00A2          00185                MOVWF   CMDO
004E   21BC          00186                CALL    SEND_C
                     00187
004F   21C6          00188                CALL    DELAY
0050   21C6          00189                CALL    DELAY
                     00190
0051   302C          00191                MOVLW   0X2C            ;VC ON, VR OFF, VF OFF
0052   00A2          00192                MOVWF   CMDO
0053   21BC          00193                CALL    SEND_C
                     00194
0054   21C6          00195                CALL    DELAY
0055   21C6          00196                CALL    DELAY

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LOC  OBJECT CODE     LINE SOURCE TEXT
  VALUE

0056   302E          00198                MOVLW   0X2E            ;VC ON, VR ON, VF OFF
0057   00A2          00199                MOVWF   CMDO
0058   21BC          00200                CALL    SEND_C
                     00201
0059   21C6          00202                CALL    DELAY
005A   21C6          00203                CALL    DELAY
                     00204
005B   302F          00205                MOVLW   0X2F            ;VC ON, VR ON, VF ON
005C   00A2          00206                MOVWF   CMDO
005D   21BC          00207                CALL    SEND_C
                     00208
005E   21C6          00209                CALL    DELAY
005F   21C6          00210                CALL    DELAY
                     00211
0060   3040          00212                MOVLW   0X40            ;INITIAL DISPLAY LINE
0061   00A2          00213                MOVWF   CMDO
0062   21BC          00214                CALL    SEND_C
                     00215
0063   30B0          00216                MOVLW   0XB0            ;PAGE
0064   00A2          00217                MOVWF   CMDO
0065   21BC          00218                CALL    SEND_C
                     00219
0066   3010          00220                MOVLW   0X10            ;COL ADDR
0067   00A2          00221                MOVWF   CMDO
0068   21BC          00222                CALL    SEND_C
                     00223
0069   3000          00224                MOVLW   0X00
006A   00A2          00225                MOVWF   CMDO
006B   21BC          00226                CALL    SEND_C
```

```
                     00227
006C   30AF          00228                MOVLW   0XAF            ;DISPLAY ON
006D   00A2          00229                MOVWF   CMDO
006E   21BC          00230                CALL    SEND_C
                     00231
                     00232
```

SUBROUTINE

```
                     00536
;*************************************************
                     00707 ;SUBROUTINE DISPLAY
                     00708 ;SEND COMMAND
                     00709 ;*************************************************
                     00710
01B2                 00711 SEND_D
01B2   1106          00712                BCF     PORTB,RW                ; WRITE DATA
01B3   1409          00713                BSF     PORTE,A0
01B4   1486          00714                BSF     PORTB,E
01B5   1286          00715                BCF     PORTB,CS1B
01B6   0824          00716                MOVF    DATAO,W
01B7   0088          00717                MOVWF   LCD_DATA
01B8   1686          00718                BSF     PORTB,CS1B
01B9   1086          00719                BCF     PORTB,E
01BA   1506          00720                BSF     PORTB,RW
01BB   0008          00721                RETURN
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LOC  OBJECT CODE     LINE SOURCE TEXT
  VALUE

                     00722
                     00723
                     00724 ;*************************************************
                     00725 ;               SEND_D SUBROUTINE
                     00726 ;*************************************************
                     00727
01BC                 00728 SEND_C
01BC   1106          00729                BCF     PORTB,RW                ; WRITE COMMAND
01BD   1009          00730                BCF     PORTE,A0
01BE   1486          00731                BSF     PORTB,E
01BF   1286          00732                BCF     PORTB,CS1B
01C0   0822          00733                MOVF    CMDO,W
01C1   0088          00734                MOVWF   LCD_DATA
01C2   1689          00735                BSF     PORTE,CS1B
01C3   1086          00736                BCF     PORTB,E
01C4   1506          00737                BSF     PORTB,RW
01C5   0008          00738                RETURN
                     00739
                     00740
```

18.0 PRECAUTION FOR HANDLING LCM

Liquid Crystal Display (LCD)

LCD is made up of glass, organic sealant, organic fluid and polymer based polarizers. The following precautions should be taken when handling.

b) Keep the temperature within the range of use and storage. Excessive temperature and humidity could cause polarization degradation, polarizer peel off or bubble.
c) Do not contact the exposed polarizer with anything harder than HB pencil lead. To clean dust off the display surface, wipe gently with cotton, chamois or other soft material soaked in petroleum benzene.
d) Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause polarizer deformation or color fading, while an active LCD with water condensation on its surface will cause corrosion of ITO electrodes.
e) Glass can be easily chipped or cracked from rough handling, especially at comers and edges.
f) Do not drive LCD with DC voltage.
g) Do not touch ITO on the contact pad and ITO traces around LSI without glove as it might cause distribution of contamination agents to the ITO.

Static Electricity

LCM contains CMOS LSI's and the same precaution for such devices should apply, namely

a) The operator should be grounded when ever he/she comes into contact with the module. Never touch any of the conductive parts such as the interface terminals with any parts of the human body.
b) The modules should be kept in antistatic bags or other containers to static for storage.
c) Only the properly grounded soldering irons should be used.
d) If an electric screwdriver is used, it should be well grounded and shielded from commutator spark.
e) The normal static prevention measures should be observed for work clothes and working benches, the latter conductive (rubber) mat is recommended.

Operation

a) The contrast can be adjusted by varying Gain and Potentiometer in the software.
b) Driving voltage should be kept within specified range, excess voltage shortens display life.
c) Response time increases with decrease in temperature.
d) Display may turn black or dark blue at temperature above its operational range, this is (however not pressing on the viewing area) may cause the segments to appear "fractured"
e) Mechanical disturbance during operation (such as pressing on the viewing area) may cause the segments to appear "fractured"

Storage

If any liquid leaks out of the damaged glass cell, wash off any human part that comes into contact with soap and water. Never swallow the fluid. The toxicity is extremely low but caution should be exercised at all time.

Limited Warranty

Unless otherwise agreed between Crystal Clear Technology and customer, Crystal Clear Technology will replace or repair any if its LCD and LCM which is found to be defective electrically and visually when inspected in accordance with Crystal Clear Technology acceptance standards, for a period of one year from date of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of Crystal Clear Technology is limited to repair and/or replacement on the terms set forth above. Crystal Clear Technology will not be responsible for any subsequent or consequential events.