

# Am73/8303 • Am73/8304B

Octal Three-State Bidirectional Bus Transceivers

## DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- $V_{CC} - 1.15V$   $V_{OH}$  interfaces with TTL, MOS and CMOS
- 48mA, 300pF bus drive capability
- Am73/8303 inverting transceivers
- Am73/8304B noninverting transceivers
- Transmit/Receive and Chip Disable simplify control logic
- 20-pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down
- 100% product assurance screening to MIL-STD-883 requirements

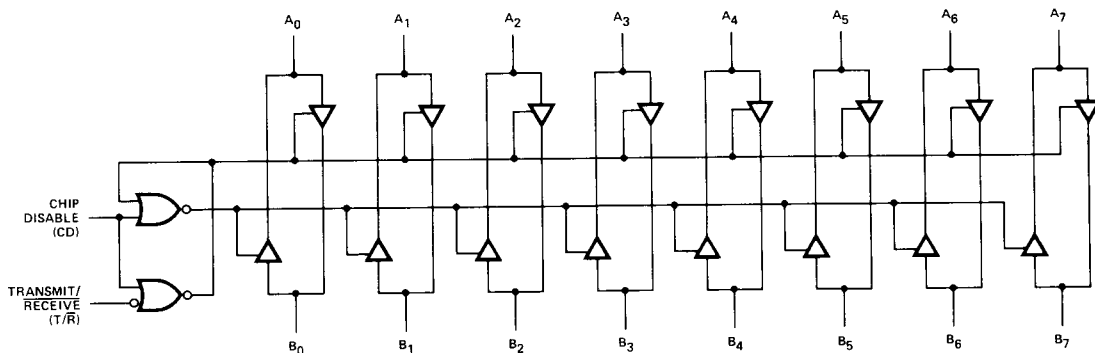
## FUNCTIONAL DESCRIPTION

The Am73/8303 and Am73/8304B are 8-bit 3-State Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 16mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

One input, Transmit/Receive determines the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a 3-state condition. Chip Disable is functionally the same as an active LOW chip select.

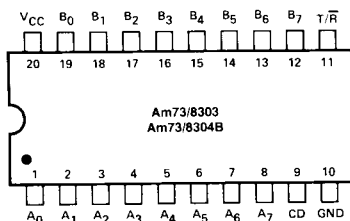
The output high voltage ( $V_{OH}$ ) is specified at  $V_{CC} - 1.15V$  minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

**Am73/8304B  
LOGIC DIAGRAM**



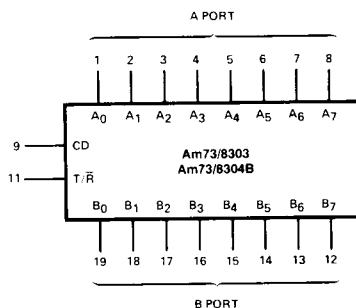
Am73/8303 has inverting transceivers

**CONNECTION DIAGRAM  
Top View**



Note: Pin 1 is marked for orientation.

**LOGIC SYMBOL**



$V_{CC}$  = Pin 20  
GND = Pin 10

**ABSOLUTE MAXIMUM RATINGS** (Above which the useful life may be impaired)

Storage Temperature	-65 to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Lead Temperature (Soldering, 10 seconds)	300°C

**ELECTRICAL CHARACTERISTICS**

The Following Conditions Apply Unless Otherwise Noted:

MIL	$T_A = -55$ to $+125^\circ\text{C}$	$V_{CC} \text{ MIN} = 4.5\text{V}$	$V_{CC} \text{ MAX} = 5.5\text{V}$
COM'L	$T_A = 0$ to $+70^\circ\text{C}$	$V_{CC} \text{ MIN} = 4.75\text{V}$	$V_{CC} \text{ MAX} = 5.25\text{V}$

**DC ELECTRICAL CHARACTERISTICS** over operating temperature range

Parameters	Description	Test Conditions	Min	Typ (Note 1)	Max	Units	
A PORT (A <sub>0</sub> -A <sub>7</sub> )							
V <sub>IH</sub>	Logical "1" Input Voltage	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 2.0V	2.0			Volts	
V <sub>IL</sub>	Logical "0" Input Voltage	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 2.0V	COM'L MIL		0.8 0.7	Volts	
V <sub>OH</sub>	Logical "1" Output Voltage	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 0.8V	I <sub>OH</sub> = -0.4mA I <sub>OH</sub> = -3.0mA	V <sub>CC</sub> -1.15 2.7	V <sub>CC</sub> -0.7 3.95	Volts	
V <sub>OL</sub>	Logical "0" Output Voltage	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 0.8V	I <sub>OL</sub> = 8mA COM'L I <sub>OL</sub> = 16mA		0.3 0.35	0.4 0.50	Volts
I <sub>OS</sub>	Output Short Circuit Current	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 0.8V, V <sub>O</sub> = 0V, V <sub>CC</sub> = MAX, Note 2	-10	-38	-75	mA	
I <sub>IH</sub>	Logical "1" Input Current	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 2.0V, V <sub>I</sub> = 2.7V		0.1	80	$\mu$ A	
I <sub>I</sub>	Input Current at Maximum Input Voltage	CD = 2.0V, V <sub>CC</sub> MAX, V <sub>I</sub> = V <sub>CC</sub> MAX			1	mA	
I <sub>IL</sub>	Logical "0" Input Current	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 2.0V, V <sub>I</sub> = 0.4V		-70	-200	$\mu$ A	
V <sub>C</sub>	Input Clamp Voltage	CD = 2.0V, I <sub>IN</sub> = -12mA		-0.7	-1.5	Volts	
I <sub>OD</sub>	Output/Input 3-State Current	CD = 2.0V	V <sub>O</sub> = 0.4V V <sub>O</sub> = 4.0V		-200 80	$\mu$ A	
B PORT (B <sub>0</sub> -B <sub>7</sub> )							
V <sub>IH</sub>	Logical "1" Input Voltage	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = V <sub>IL</sub> MAX	2.0			Volts	
V <sub>IL</sub>	Logical "0" Input Voltage	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = V <sub>IL</sub> MAX	COM'L MIL		0.8 0.7	Volts	
V <sub>OH</sub>	Logical "1" Output Voltage	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 2.0V	I <sub>OH</sub> = -0.4mA I <sub>OH</sub> = -5.0mA I <sub>OH</sub> = -10mA	V <sub>CC</sub> -1.15 2.7 2.4	V <sub>CC</sub> -0.8 3.9 3.6	Volts	
V <sub>OL</sub>	Logical "0" Output Voltage	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 2.0V	I <sub>OL</sub> = 20mA I <sub>OL</sub> = 48mA		0.3 0.4	0.4 0.5	Volts
I <sub>OS</sub>	Output Short Circuit Current	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 2.0V, V <sub>O</sub> = 0V V <sub>CC</sub> = MAX, Note 2	-25	-50	-150	mA	
I <sub>IH</sub>	Logical "1" Input Current	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = V <sub>IL</sub> MAX, V <sub>I</sub> = 2.7V		0.1	80	$\mu$ A	
I <sub>I</sub>	Input Current at Maximum Input Voltage	CD = 2.0V, V <sub>CC</sub> = MAX, V <sub>I</sub> = V <sub>CC</sub> MAX			1	mA	
I <sub>IL</sub>	Logical "0" Input Current	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = V <sub>IL</sub> MAX, V <sub>I</sub> = 0.4V		-70	-200	$\mu$ A	
V <sub>C</sub>	Input Clamp Voltage	CD = 2.0V, I <sub>IN</sub> = -12mA		-0.7	-1.5	Volts	
I <sub>OD</sub>	Output/Input 3-State Current	CD = 2.0V	V <sub>O</sub> = 0.4V V <sub>O</sub> = 4.0V		-200 200	$\mu$ A	
CONTROL INPUTS CD, T/ $\bar{R}$							
V <sub>IH</sub>	Logical "1" Input Voltage		2.0			Volts	
V <sub>IL</sub>	Logical "0" Input Voltage		COM'L MIL		0.8 0.7	Volts	
I <sub>IH</sub>	Logical "1" Input Current	V <sub>I</sub> = 2.7V		0.5	20	$\mu$ A	
I <sub>I</sub>	Input Current at Maximum Input Voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = V <sub>CC</sub> MAX			1.0	mA	
I <sub>IL</sub>	Logical "0" Input Current	V <sub>I</sub> = 0.4V	T/ $\bar{R}$ CD	-0.1 -0.1	-0.25 -0.25	mA	
V <sub>C</sub>	Input Clamp Voltage	I <sub>IN</sub> = -12mA		-0.8	-1.5	Volts	
POWER SUPPLY CURRENT							
I <sub>CC</sub>	Power Supply Current	Am73/8303	CD = V <sub>I</sub> = 2.0V, V <sub>CC</sub> = MAX	70	100	mA	
			CD = 0.4V, V <sub>INA</sub> = T/ $\bar{R}$ = 2.0V, V <sub>CC</sub> = MAX	100	150		
		Am73/8304B	CD = 2.0V, V <sub>I</sub> = 0.4V, V <sub>CC</sub> = MAX	70	100	mA	
			CD = V <sub>INA</sub> = 0.4V, T/ $\bar{R}$ = 2.0V, V <sub>CC</sub> = MAX	90	140		

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0V$ ,  $T_A = 25^\circ C$ )

Parameters	Description	Test Conditions	Typ (Note 1)	Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t <sub>PDHLA</sub>	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/ $\bar{R}$ = 0.4V (Figure 1) R <sub>1</sub> = 1k, R <sub>2</sub> = 5k, C <sub>1</sub> = 30pF	8	12	ns
t <sub>PDLHA</sub>	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/ $\bar{R}$ = 0.4V (Figure 1) R <sub>1</sub> = 1k, R <sub>2</sub> = 5k, C <sub>1</sub> = 30pF	11	16	ns
t <sub>PLZA</sub>	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B <sub>0</sub> to B <sub>7</sub> = 2.4V, T/ $\bar{R}$ = 0.4V (Figure 3) S <sub>3</sub> = 1, R <sub>5</sub> = 1k, C <sub>4</sub> = 15pF	10	15	ns
t <sub>PHZA</sub>	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B <sub>0</sub> to B <sub>7</sub> = 0.4V, T/ $\bar{R}$ = 0.4V (Figure 3) S <sub>3</sub> = 0, R <sub>5</sub> = 1k, C <sub>4</sub> = 15pF	8	15	ns
t <sub>PZLA</sub>	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B <sub>0</sub> to B <sub>7</sub> = 2.4V, T/ $\bar{R}$ = 0.4V (Figure 3) S <sub>3</sub> = 1, R <sub>5</sub> = 1k, C <sub>4</sub> = 30pF	20	30	ns
t <sub>PZHA</sub>	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B <sub>0</sub> to B <sub>7</sub> = 0.4V, T/ $\bar{R}$ = 0.4V (Figure 3) S <sub>3</sub> = 0, R <sub>5</sub> = 5k, C <sub>4</sub> = 30pF	19	30	ns
B PORT DATA/MODE SPECIFICATIONS					
t <sub>PDHLB</sub>	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/ $\bar{R}$ = 2.4V (Figure 1) R <sub>1</sub> = 100Ω, R <sub>2</sub> = 1k, C <sub>1</sub> = 300pF	12	18	ns
		R <sub>1</sub> = 667Ω, R <sub>2</sub> = 5k, C <sub>1</sub> = 45pF	7	12	ns
t <sub>PDLHB</sub>	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/ $\bar{R}$ = 2.4V (Figure 1) R <sub>1</sub> = 100Ω, R <sub>2</sub> = 1k, C <sub>1</sub> = 300pF	15	20	ns
		R <sub>1</sub> = 667Ω, R <sub>2</sub> = 5k, C <sub>1</sub> = 45pF	9	14	ns
t <sub>PLZB</sub>	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A <sub>0</sub> to A <sub>7</sub> = 2.4V, T/ $\bar{R}$ = 2.4V (Figure 3) S <sub>3</sub> = 1, R <sub>5</sub> = 1k, C <sub>4</sub> = 15pF	13	18	ns
t <sub>PHZB</sub>	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A <sub>0</sub> to A <sub>7</sub> = 0.4V, T/ $\bar{R}$ = 2.4V (Figure 3) S <sub>3</sub> = 0, R <sub>5</sub> = 1k, C <sub>4</sub> = 15pF	8	15	ns
t <sub>PZLB</sub>	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A <sub>0</sub> to A <sub>7</sub> = 2.4V, T/ $\bar{R}$ = 2.4V (Figure 3) S <sub>3</sub> = 1, R <sub>5</sub> = 100Ω, C <sub>4</sub> = 300pF	25	35	ns
		S <sub>3</sub> = 1, R <sub>5</sub> = 667Ω, C <sub>4</sub> = 45pF	16	25	ns
t <sub>PZHB</sub>	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A <sub>0</sub> to A <sub>7</sub> = 0.4V, T/ $\bar{R}$ = 2.4V (Figure 3) S <sub>3</sub> = 0, R <sub>5</sub> = 1k, C <sub>4</sub> = 300pF	22	35	ns
		S <sub>3</sub> = 0, R <sub>5</sub> = 5k, C <sub>4</sub> = 45pF	14	25	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t <sub>TRL</sub>	Propagation Delay from Transmit Mode to Receive a Logical "0", T/ $\bar{R}$ to A Port	CD = 0.4V (Figure 2) S <sub>1</sub> = 1, R <sub>4</sub> = 100Ω, C <sub>3</sub> = 5pF S <sub>2</sub> = 1, R <sub>3</sub> = 1k, C <sub>2</sub> = 30pF	23	35	ns
t <sub>TRH</sub>	Propagation Delay from Transmit Mode to Receive a Logical "1", T/ $\bar{R}$ to A Port	CD = 0.4V (Figure 2) S <sub>1</sub> = 0, R <sub>4</sub> = 100Ω, C <sub>3</sub> = 5pF S <sub>2</sub> = 0, R <sub>3</sub> = 5k, C <sub>2</sub> = 30pF	22	35	ns
t <sub>RTL</sub>	Propagation Delay from Receive Mode to Transmit a Logical "0", T/ $\bar{R}$ to B Port	CD = 0.4V (Figure 2) S <sub>1</sub> = 1, R <sub>4</sub> = 100Ω, C <sub>3</sub> = 300pF S <sub>2</sub> = 1, R <sub>3</sub> = 300Ω, C <sub>2</sub> = 5pF	26	35	ns
t <sub>RTH</sub>	Propagation Delay from Receive Mode to Transmit a Logical "1", T/ $\bar{R}$ to B Port	CD = 0.4V (Figure 2) S <sub>1</sub> = 0, R <sub>4</sub> = 1k, C <sub>3</sub> = 300pF S <sub>2</sub> = 0, R <sub>3</sub> = 300Ω, C <sub>2</sub> = 5pF	27	35	ns

Notes: 1. All typical values given are for  $V_{CC} = 5.0V$  and  $T_A = 25^\circ C$ .

2. Only one output at a time should be shorted.

**FUNCTION TABLE**

Inputs	Conditions		
Chip Disable	0	0	1
Transmit/Receive	0	1	X
A Port	Out	In	HI-Z
B Port	In	Out	HI-Z

# AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0V$ , $T_A = 25^\circ C$ )

Parameters	Description	Test Conditions	Typ (Note 1)	Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t <sub>PDHLA</sub>	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/ $\bar{R}$ = 0.4V (Figure 1) R <sub>1</sub> = 1k, R <sub>2</sub> = 5k, C <sub>1</sub> = 30pF	14	18	ns
t <sub>PDLHA</sub>	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/ $\bar{R}$ = 0.4V (Figure 1) R <sub>1</sub> = 1k, R <sub>2</sub> = 5k, C <sub>1</sub> = 30pF	13	18	ns
t <sub>PLZA</sub>	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B <sub>0</sub> to B <sub>7</sub> = 0.4V, T/ $\bar{R}$ = 0.4V (Figure 3) S <sub>3</sub> = 1, R <sub>5</sub> = 1k, C <sub>4</sub> = 15pF	11	15	ns
t <sub>PHZA</sub>	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B <sub>0</sub> to B <sub>7</sub> = 2.4V, T/ $\bar{R}$ = 0.4V (Figure 3) S <sub>3</sub> = 0, R <sub>5</sub> = 1k, C <sub>4</sub> = 15pF	8	15	ns
t <sub>PZLA</sub>	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B <sub>0</sub> to B <sub>7</sub> = 0.4V, T/ $\bar{R}$ = 0.4V (Figure 3) S <sub>3</sub> = 1, R <sub>5</sub> = 1k, C <sub>4</sub> = 30pF	27	35	ns
t <sub>PZHA</sub>	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B <sub>0</sub> to B <sub>7</sub> = 2.4V, T/ $\bar{R}$ = 0.4V (Figure 3) S <sub>3</sub> = 0, R <sub>5</sub> = 5k, C <sub>4</sub> = 30pF	19	25	ns
B PORT DATA/MODE SPECIFICATIONS					
t <sub>PDHLB</sub>	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/ $\bar{R}$ = 2.4V (Figure 1)	18	23	ns
		R <sub>1</sub> = 100Ω, R <sub>2</sub> = 1k, C <sub>1</sub> = 300pF			
		R <sub>1</sub> = 667Ω, R <sub>2</sub> = 5k, C <sub>1</sub> = 45pF			
t <sub>PDLHB</sub>	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/ $\bar{R}$ = 2.4V (Figure 1)	16	23	ns
		R <sub>1</sub> = 100Ω, R <sub>2</sub> = 1k, C <sub>1</sub> = 300pF			
		R <sub>1</sub> = 667Ω, R <sub>2</sub> = 5k, C <sub>1</sub> = 45pF			
t <sub>PLZB</sub>	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A <sub>0</sub> to A <sub>7</sub> = 0.4V, T/ $\bar{R}$ = 2.4V (Figure 3) S <sub>3</sub> = 1, R <sub>5</sub> = 1k, C <sub>4</sub> = 15pF	13	18	ns
t <sub>PHZB</sub>	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A <sub>0</sub> to A <sub>7</sub> = 2.4V, T/ $\bar{R}$ = 2.4V (Figure 3) S <sub>3</sub> = 0, R <sub>5</sub> = 1k, C <sub>4</sub> = 15pF	8	15	ns
t <sub>PZLB</sub>	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A <sub>0</sub> to A <sub>7</sub> = 0.4V, T/ $\bar{R}$ = 2.4V (Figure 3)	32	40	ns
		S <sub>3</sub> = 1, R <sub>5</sub> = 100Ω, C <sub>4</sub> = 300pF			
		S <sub>3</sub> = 1, R <sub>5</sub> = 667Ω, C <sub>4</sub> = 45pF			
t <sub>PZHB</sub>	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A <sub>0</sub> to A <sub>7</sub> = 2.4V, T/ $\bar{R}$ = 2.4V (Figure 3)	26	35	ns
		S <sub>3</sub> = 0, R <sub>5</sub> = 1k, C <sub>4</sub> = 300pF			
		S <sub>3</sub> = 0, R <sub>5</sub> = 5k, C <sub>4</sub> = 45pF			
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t <sub>TRL</sub>	Propagation Delay from Transmit Mode to Receive a Logical "0", T/ $\bar{R}$ to A Port	CD = 0.4V (Figure 2) S <sub>1</sub> = 0, R <sub>4</sub> = 100Ω, C <sub>3</sub> = 5pF S <sub>2</sub> = 1, R <sub>3</sub> = 1k, C <sub>2</sub> = 30pF	30	40	ns
t <sub>TRH</sub>	Propagation Delay from Transmit Mode to Receive a Logical "1", T/ $\bar{R}$ to A Port	CD = 0.4V (Figure 2) S <sub>1</sub> = 1, R <sub>4</sub> = 100Ω, C <sub>3</sub> = 5pF S <sub>2</sub> = 0, R <sub>3</sub> = 5k, C <sub>2</sub> = 30pF	28	40	ns
t <sub>RTL</sub>	Propagation Delay from Receive Mode to Transmit a Logical "0", T/ $\bar{R}$ to B Port	CD = 0.4V (Figure 2) S <sub>1</sub> = 1, R <sub>4</sub> = 100Ω, C <sub>3</sub> = 300pF S <sub>2</sub> = 0, R <sub>3</sub> = 300Ω, C <sub>2</sub> = 5pF	31	40	ns
t <sub>RTH</sub>	Propagation Delay from Receive Mode to Transmit a Logical "1", T/ $\bar{R}$ to B Port	CD = 0.4V (Figure 2) S <sub>1</sub> = 0, R <sub>4</sub> = 1k, C <sub>3</sub> = 300pF S <sub>2</sub> = 1, R <sub>3</sub> = 300Ω, C <sub>2</sub> = 5pF	28	40	ns

Notes: 1. All typical values given are for  $V_{CC} = 5.0V$  and  $T_A = 25^\circ C$ .  
2. Only one output at a time should be shorted.

## DEFINITION OF FUNCTIONAL TERMS

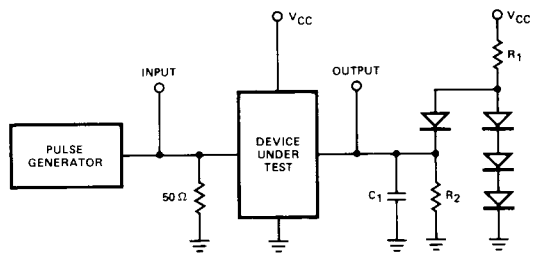
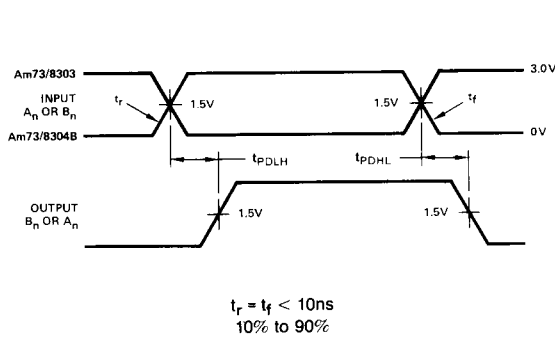
**A<sub>0</sub>-A<sub>7</sub>** A port inputs/outputs are receiver output drivers when  $T/\bar{R}$  is LOW and are transmit inputs when  $T/\bar{R}$  is HIGH.

**B<sub>0</sub>-B<sub>7</sub>** B port inputs/outputs are transmit output drivers when  $T/\bar{R}$  is HIGH and receiver inputs when  $T/\bar{R}$  is LOW.

**CD** Chip Disable forces all output drivers into 3-state when HIGH (same function as active LOW chip select,  $\bar{CS}$ ).

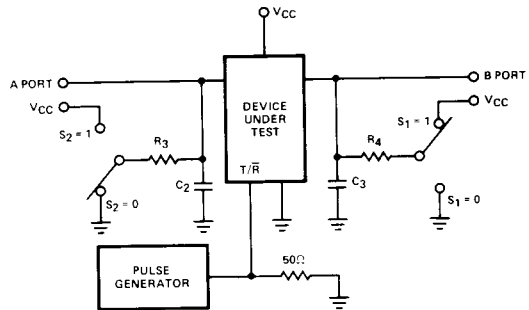
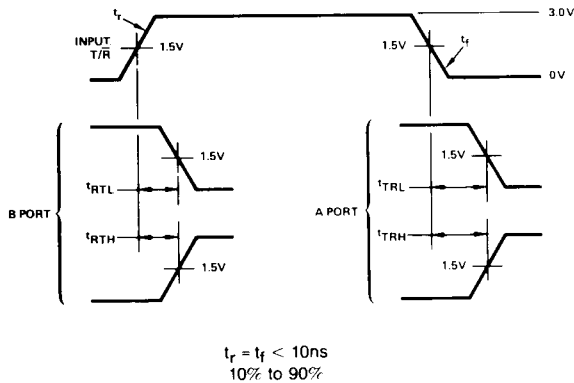
**$T/\bar{R}$**  Transmit/Receive direction control determines whether A port or B port drivers are in 3-state. With  $T/\bar{R}$  HIGH A port is the input and B port is the output. With  $T/\bar{R}$  LOW A port is the output and B port is the input.

# SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS



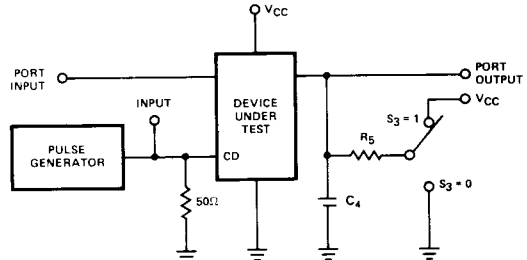
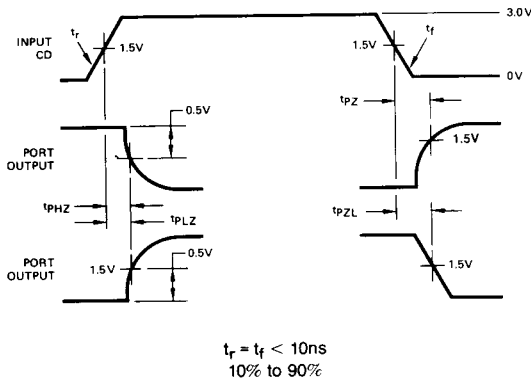
Note:  $C_1$  includes test fixture capacitance.

Figure 1. Propagation Delay from A Port to B Port  
or from B Port to A Port.



Note:  $C_2$  and  $C_3$  include test fixture capacitance.

Figure 2. Propagation Delay from  $T/\bar{R}$  to A Port or B Port.

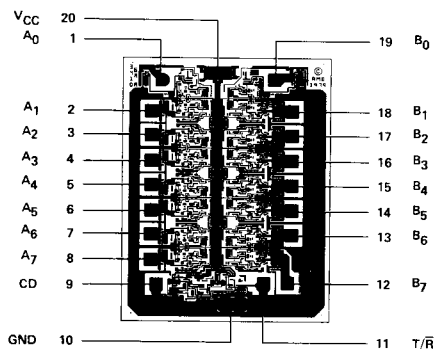


Note:  $C_4$  includes test fixture capacitance.  
Port input is in a fixed logical condition.

Figure 3. Propagation Delay from CD to A Port or B Port.

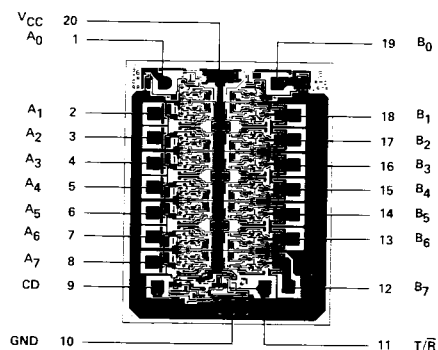
## Metallization and Pad Layouts

Am73/8303



DIE SIZE .069" X .089"

Am73/8304B



DIE SIZE .069" X .089"

## ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am73/8303 Order Number	Am73/8304B Order Number	Package Type (Note 1)	Operating (Note 2)	Screening Level (Note 3)
DP7303J	DP7304BJ	D-20	M	C-3
DP7303JB	DP7304BJB	D-20	M	B-3
DP8303J	DP8304BJ	D-20	C	C-1
DP8303JB	DP8304BJB	D-20	C	B-1
DP8303N	DP8304BN	P-20	C	C-1
DP8303NB	DP8304BNB	P-20	C	B-1
AM7303X	AM7304BX	Dice	M	Visual inspection to MIL-STD-883 Method 2010B.
AM8303X	AM8304BX	Dice	C	

## Notes:

1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads.
2. C = 0 to 70°C, V<sub>CC</sub> = 4.75 to 5.25V, M = -55 to +125°C, V<sub>CC</sub> = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.