FAIRCHILD

SEMICONDUCTOR ™

DM74LS243
Quadruple Bus Transceiver

General Description

This four data line transceiver is designed for asynchronous two-way communications between data buses. It can be used to drive terminated lines down to 133Ω.

Features

- Two-way asynchronous communication between data buses
- PNP inputs reduce DC loading on bus line
- Hysteresis at data inputs improves noise margin

Ordering Code:

Order Number	Package Number	Package Description
DM74LS243M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS243N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram
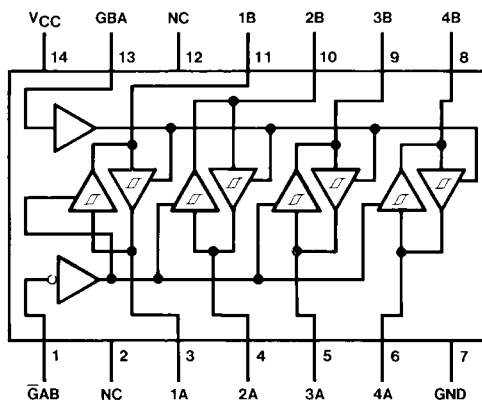
Function Table

Control Inputs		Data Port Status	
$\overline{G}$ AB	GBA	A	B
H	H	O	I
L	H	(Note 1)	(Note 1)
H	L	ISOLATED	
L	L	I	O

I = Input
O = Output
H = HIGH Logic Level
L = LOW Logic Level

Note 1: Possibly destructive oscillation may occur if the transceivers are enabled in both directions at once.

Absolute Maximum Ratings(Note 2)

Supply Voltage	7V
Input Voltage	
Any G	7V
A or B	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−15	mA
I_{OL}	LOW Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics
over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$) (Data Inputs Only)	V_{CC} = Min		0.2	0.4		V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −1 mA		2.7			V
		V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −3 mA		2.4	3.4		
		V_{CC} = Min, V_{IH} = Min V_{IL} = 0.5V, I_{OH} = Max		2			
V_{OL}	LOW Level Output Voltage	V_{CC} = Min V_{IL} = Max V_{IH} = Min	I_{OL} = 12 mA I_{OL} = Max			0.4 0.5	V
I_{OZH}	Off-State Output Current, HIGH Level Voltage Applied	V_{CC} = Max V_{IL} = Max	V_O = 2.7V			40	µA
I_{OZL}	Off-State Output Current, LOW Level Voltage Applied	V_{IH} = Min	V_O = 0.4V			−200	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V A or B			0.1	mA
			V_I = 7V Any G			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)		−40		−225	mA
I_{CC}	Supply Current	V_{CC} = Max Outputs OPEN	Outputs HIGH		22	38	mA
			Outputs LOW		29	50	
			Outputs Disabled		32	54	

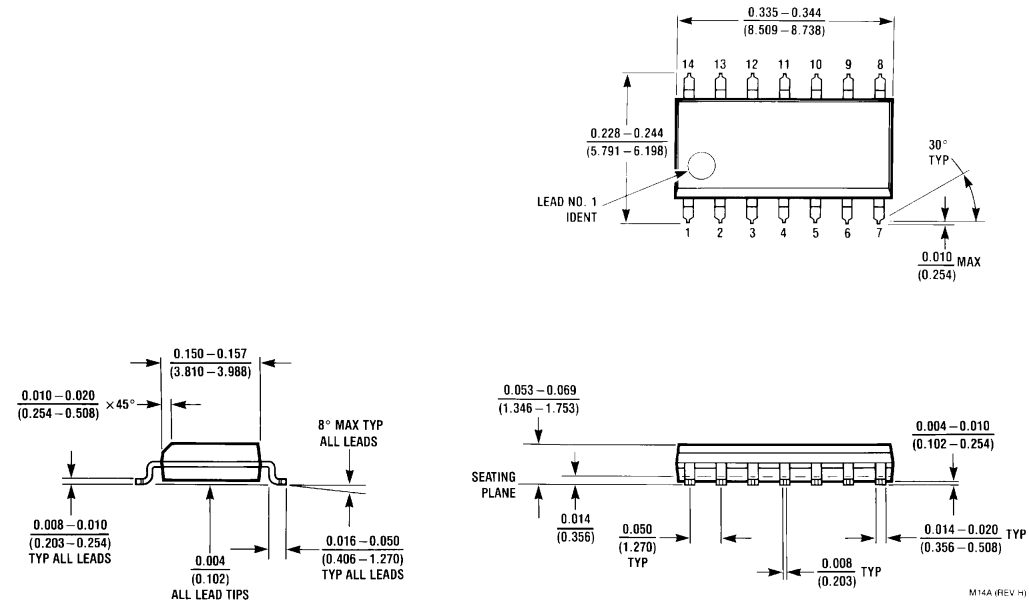**Note 3:** All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

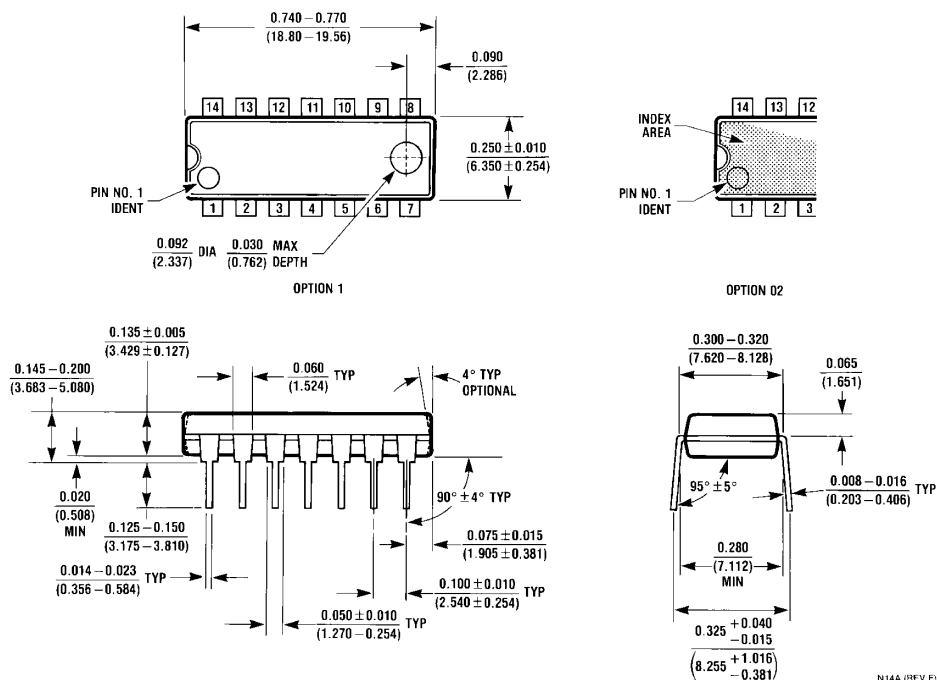## Switching Characteristics

at $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	$C_L = 45$ pF $R_L = 667\Omega$		18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	$C_L = 45$ pF $R_L = 667\Omega$		18	ns
t_{PZL}	Output Enable Time to LOW Level	$C_L = 45$ pF $R_L = 667\Omega$		30	ns
t_{PZH}	Output Enable Time to HIGH Level	$C_L = 45$ pF $R_L = 667\Omega$		23	ns
t_{PLZ}	Output Disable Time from LOW Level	$C_L = 5$ pF $R_L = 667\Omega$		25	ns
t_{PHZ}	Output Disable Time from HIGH Level	$C_L = 5$ pF $R_L = 667\Omega$		18	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	$C_L = 150$ pF $R_L = 667\Omega$		21	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	$C_L = 150$ pF $R_L = 667\Omega$		22	ns
t_{PZL}	Output Enable Time to LOW Level	$C_L = 150$ pF $R_L = 667\Omega$		33	ns
t_{PZH}	Output Enable Time to HIGH Level	$C_L = 150$ pF $R_L = 667\Omega$		26	ns

Physical Dimensions inches (millimeters) unless otherwise noted

$\dfrac{0.335 - 0.344}{(8.509 - 8.738)}$

14 13 12 11 10 9 8

$\dfrac{0.228 - 0.244}{(5.791 - 6.198)}$

LEAD NO. 1
IDENT

1 2 3 4 5 6 7

30°
TYP

$\dfrac{0.010}{(0.254)}$ MAX

$\dfrac{0.150 - 0.157}{(3.810 - 3.988)}$

$\dfrac{0.010 - 0.020}{(0.254 - 0.508)} \times 45°$

8° MAX TYP
ALL LEADS

$\dfrac{0.008 - 0.010}{(0.203 - 0.254)}$
TYP ALL LEADS

$\dfrac{0.004}{(0.102)}$
ALL LEAD TIPS

$\dfrac{0.016 - 0.050}{(0.406 - 1.270)}$
TYP ALL LEADS

$\dfrac{0.053 - 0.069}{(1.346 - 1.753)}$

$\dfrac{0.004 - 0.010}{(0.102 - 0.254)}$

SEATING
PLANE

$\dfrac{0.014}{(0.356)}$

$\dfrac{0.050}{(1.270)}$
TYP

$\dfrac{0.008}{(0.203)}$ TYP

$\dfrac{0.014 - 0.020}{(0.356 - 0.508)}$ TYP

M14A (REV H)

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.740 − 0.770
(18.80 − 19.56)

0.090
(2.286)

14 13 12 11 10 9 8

0.250 ± 0.010
(6.350 ± 0.254)

PIN NO. 1
IDENT

1 2 3 4 5 6 7

0.092
(2.337) DIA   0.030 MAX
(0.762) DEPTH

OPTION 1

INDEX
AREA

14 13 12

PIN NO. 1
IDENT

1 2 3

OPTION 02

0.135 ± 0.005
(3.429 ± 0.127)

0.145 − 0.200
(3.683 − 5.080)

0.060
(1.524) TYP

4° TYP
OPTIONAL

0.020
(0.508)
MIN

0.125 − 0.150
(3.175 − 3.810)

90° ± 4° TYP

0.075 ± 0.015
(1.905 ± 0.381)

0.014 − 0.023
(0.356 − 0.584) TYP

0.100 ± 0.010
(2.540 ± 0.254) TYP

0.050 ± 0.010
(1.270 − 0.254) TYP

0.300 − 0.320
(7.620 − 8.128)

0.065
(1.651)

95° ± 5°

0.008 − 0.016
(0.203 − 0.406) TYP

0.280
(7.112)
MIN

$0.325 \begin{smallmatrix} +0.040 \\ -0.015 \end{smallmatrix}$

$\left(8.255 \begin{smallmatrix} +1.016 \\ -0.381 \end{smallmatrix}\right)$

N14A (REV F)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

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