

CMOS Programmable Timer High Voltage Types (20V Rating)

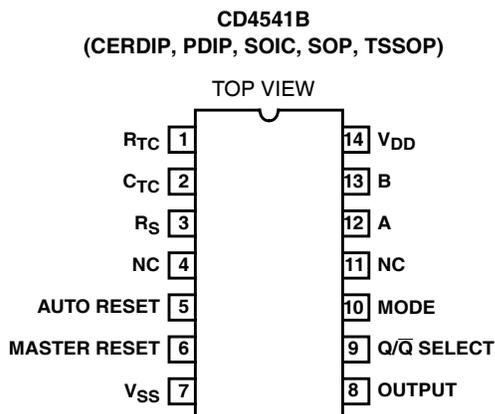
Features

- Low Symmetrical Output Resistance, Typically 100Ω at V_{DD} = 15V
- Built-In Low-Power RC Oscillator
- Oscillator Frequency Range DC to 100kHz
- External Clock (Applied to Pin 3) can be Used Instead of Oscillator
- Operates as 2^N Frequency Divider or as a Single-Transition Timer
- Q/ \bar{Q} Select Provides Output Logic Level Flexibility
- AUTO or MASTER RESET Disables Oscillator During Reset to Reduce Power Dissipation
- Operates With Very Slow Clock Rise and Fall Times
- Capable of Driving Six Low Power TTL Loads, Three Low-Power Schottky Loads, or Six HTL Loads Over the Rated Temperature Range
- Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- 5V, 10V, and 15V Parametric Ratings
- Meets All Requirements of JEDEC Standard No. 13B, “Standard Specifications for Description of ‘B’ Series CMOS Devices”

Description

CD4541B programmable timer consists of a 16-stage binary counter, an oscillator that is controlled by external R-C components (2 resistors and a capacitor), an automatic power-on reset circuit, and output control logic. The counter increments on positive-edge clock transitions and can also be reset via the MASTER RESET input.

Pinout



The output from this timer is the Q or \bar{Q} output from the 8th, 10th, 13th, or 16th counter stage. The desired stage is chosen using time-select inputs A and B (see Frequency Select Table).

The output is available in either of two modes selectable via the MODE input, pin 10 (see Truth Table). When this MODE input is a logic “1”, the output will be a continuous square wave having a frequency equal to the oscillator frequency divided by 2^N. With the MODE input set to logic “0” and after a MASTER RESET is initiated, the output (assuming Q output has been selected) changes from a low to a high state after 2^{N-1} counts and remains in that state until another MASTER RESET pulse is applied or the MODE input is set to a logic “1”.

Timing is initialized by setting the AUTO RESET input (pin 5) to logic “0” and turning power on. If pin 5 is set to logic “1”, the AUTO RESET circuit is disabled and counting will not start until after a positive MASTER RESET pulse is applied and returns to a low level. The AUTO RESET consumes an appreciable amount of power and should not be used if low-power operation is desired. For reliable automatic power-on reset, V_{DD} should be greater than 5V.

The RC oscillator, shown in Figure 2, oscillates with a frequency determined by the RC network and is calculated using:

$$f = \frac{1}{2.3 R_{TC} C_{TC}}$$

Where f is between 1kHz and 100kHz and R_S ≥ 10kΩ and ≈ 2R_{TC}

Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE |
|-------------|------------------|--------------|
| CD4541BF3A | -55 to 125 | 14 Ld CERDIP |
| CD4541BE | -55 to 125 | 14 Ld PDIP |
| CD4541BM | -55 to 125 | 14 Ld SOIC |
| CD4541BMT | -55 to 125 | 14 Ld SOIC |
| CD4541BM96 | -55 to 125 | 14 Ld SOIC |
| CD4541BNSR | -55 to 125 | 14 Ld SOP |
| CD4541BPW | -55 to 125 | 14 Ld TSSOP |
| CD4541BPWR | -55 to 125 | 14 Ld TSSOP |

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

CD4541B

Functional Diagram

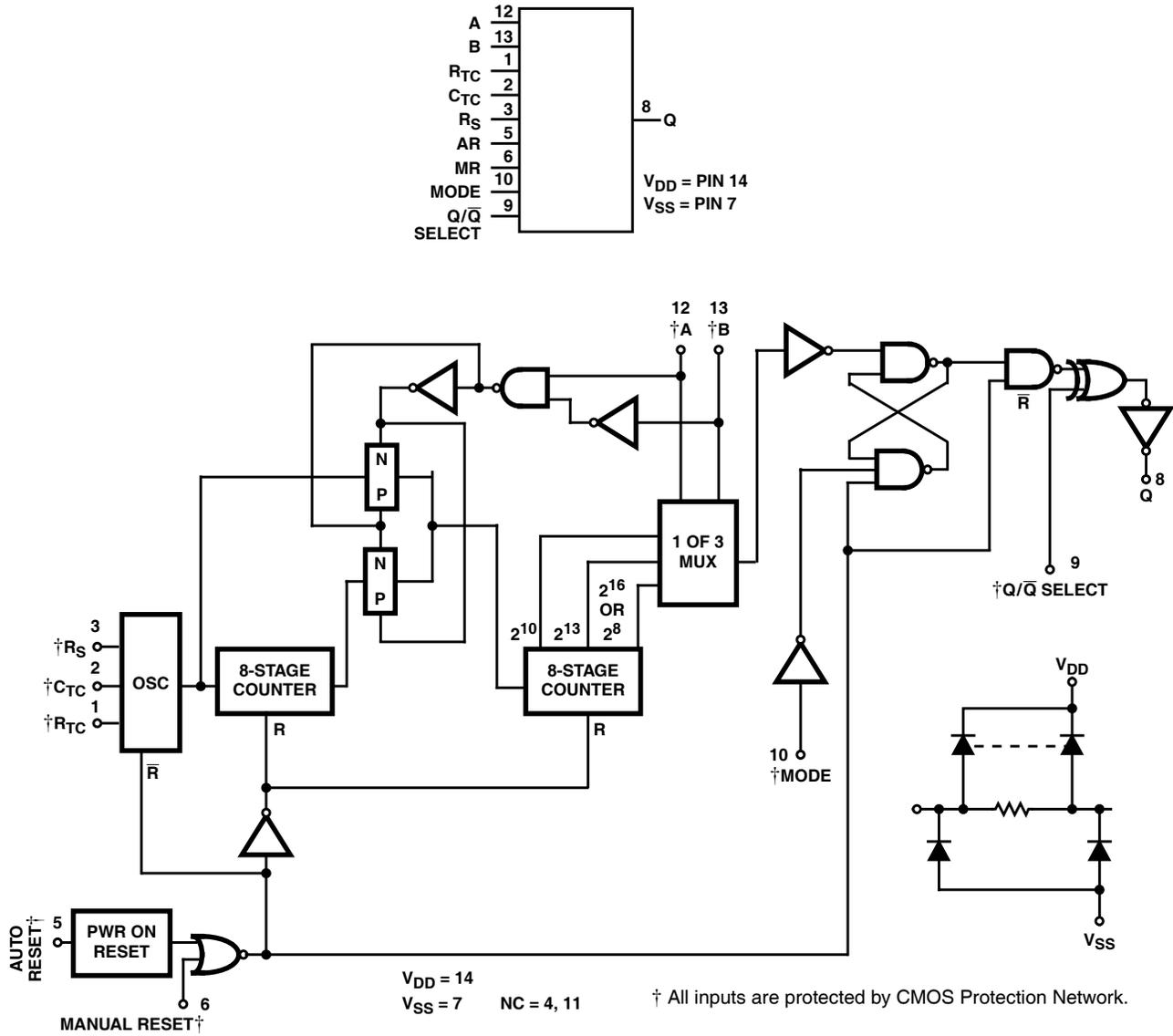


FIGURE 1.

FREQUENCY SELECTION TABLE

| A | B | NO. OF STAGES N | COUNT 2^N |
|---|---|-----------------|-------------|
| 0 | 0 | 13 | 8192 |
| 0 | 1 | 10 | 1024 |
| 1 | 0 | 8 | 256 |
| 1 | 1 | 16 | 65536 |

TRUTH TABLE

| PIN | STATE | |
|-----|--------------------------------------|---|
| | 0 | 1 |
| 5 | Auto Reset On | Auto Reset Disable |
| 6 | Master Reset Off | Master Reset On |
| 9 | Output Initially Low After Reset (Q) | Output Initially High After Reset (\bar{Q}) |
| 10 | Single Transition Mode | Recycle Mode |

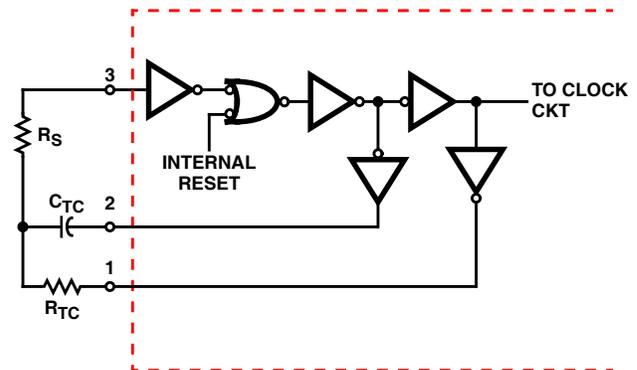


FIGURE 2. RC OSCILLATOR CIRCUIT

CD4541B

Absolute Maximum Ratings

DC Supply - Voltage Range, V_{DD}
 Voltages Referenced to V_{SS} Terminal -0.5V to +20V
 Input Voltage Range, All Inputs -0.5V to $V_{DD} + 0.5V$
 DC Input Current, Any One Input $\pm 10mA$
 Device Dissipation Per Output Transistor
 For T_A = Full Package Temperature Range
 (All Package Types) 100mW

Operating Conditions

Temperature Range T_A -55°C to 125°C
 Supply Voltage Range
 For T_A = Full Package Temperature Range 3V (Min), 18V (Typ)

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 1)
 PDIP package 80°C/W
 SOIC package 86°C/W
 SOP package 76°C/W
 TSSOP package 113°C/W
 Maximum Junction Temperature (Plastic Package) 150°C
 Maximum Storage Temperature Range (T_{STG}) -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s)
 At Distance 1/16in \pm 1/32in (1.59mm \pm 0.79mm)
 from case for 10s Maximum 265°C
 (SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Specifications

| PARAMETER | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|---|--------------|-----------------|-----------------|---------------------------------------|-------|-------|-------|-------|------|------|---------|
| | V_O (V) | V_{IN} (V) | V_{DD} (V) | -55 | -40 | 85 | 125 | 25 | | | |
| | | | | | | | | MIN | TYP | MAX | |
| Quiescent Device Current, (Note 2) I_{DD} (Max) | - | 0, 5 | 5 | 5 | 5 | 150 | 150 | - | 0.04 | 5 | μA |
| | - | 0, 10 | 10 | 10 | 10 | 300 | 300 | - | 0.04 | 10 | μA |
| | - | 0, 15 | 15 | 20 | 20 | 600 | 600 | - | 0.04 | 20 | μA |
| | - | 0, 20 | 20 | 100 | 100 | 3000 | 3000 | - | 0.08 | 100 | μA |
| Output Low (Sink) Current I_{OL} (Min) | 0.4 | 0, 5 | 5 | 1.9 | 1.85 | 1.26 | 1.08 | 1.55 | 3.1 | - | mA |
| | 0.5 | 0, 10 | 10 | 5 | 4.8 | 3.3 | 2.8 | 4 | 8 | - | mA |
| | 1.5 | 0, 15 | 15 | 12.6 | 12 | 8.4 | 7.2 | 10 | 20 | - | mA |
| Output High (Source) Current, I_{OH} (Min) | 4.6 | 0, 5 | 5 | -1.9 | -1.85 | -1.26 | -1.08 | -1.55 | -3.1 | - | mA |
| | 2.5 | 0, 5 | 5 | -6.2 | -6 | -4.1 | -3 | -5 | -10 | - | mA |
| | 9.5 | 0, 10 | 10 | -5 | -4.8 | -3.3 | -2.8 | -4 | -8 | - | mA |
| | 13.5 | 0, 15 | 15 | -12.6 | -12 | -8.4 | -7.2 | -10 | -20 | - | mA |
| Output Voltage: Low-Level, V_{OL} (Max) | - | 0, 5 | 5 | - | | 0.05 | | - | 0 | 0.05 | V |
| | - | 0, 10 | 10 | - | | 0.05 | | - | 0 | 0.05 | V |
| | - | 0, 15 | 15 | - | | 0.05 | | - | 0 | 0.05 | V |
| Output Voltage: High-Level, V_{OH} (Min) | - | 0, 5 | 5 | - | | 4.95 | | 4.95 | 5 | - | V |
| | - | 0, 10 | 10 | - | | 9.95 | | 9.95 | 10 | - | V |
| | - | 0, 15 | 15 | - | | 14.95 | | 14.95 | 15 | - | V |
| Input Low Voltage, V_{IL} (Max) | 0.5, 4.5 | - | 5 | - | | 1.5 | | - | - | 1.5 | V |
| | 1, 9 | - | 10 | - | | 3 | | - | - | 3 | V |
| | 1.5, 13.5 | - | 15 | - | | 4 | | - | - | 4 | V |

CD4541B

Electrical Specifications (Continued)

| PARAMETER | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|---|-----------------------|------------------------|------------------------|---------------------------------------|------|-----|-----|-----|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | -55 | -40 | 85 | 125 | 25 | | | |
| | | | | | | | | MIN | TYP | MAX | |
| Input High Voltage, V _{IH} (Min) | 0.5, 4.5 | - | 5 | - | | 3.5 | | 3.5 | - | - | V |
| | 1, 9 | - | 10 | - | | 7 | | 7 | - | - | V |
| | 1.5, 13.5 | - | 15 | - | | 11 | | 11 | - | - | V |
| Input Current, I _{IN} (Max) | - | 0, 18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | - | ±10 ⁻⁵ | ±0.1 | μA |

NOTE:

2. With AUTO RESET enabled, additional current drain at 25°C is:
 7μA (Typ), 200μA (Max) at 5V;
 30μA (Typ), 350μA (Max) at 10V;
 80μA (Typ), 500μA (Max) at 15V

Dynamic Electrical Specifications $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ns}$, $C_L = 50\text{pF}$, $R_L = 200\text{k}\Omega$

| PARAMETER | SYMBOL | V _{DD} (V) | MIN | TYP | MAX | UNITS |
|--|--|---------------------|-----------|------|------|-------|
| Propagation Delay Times Clock to Q | (2 ⁸) t _{PHL} , t _{PLH} | 5 | - | 3.5 | 10.5 | μs |
| | | 10 | - | 1.25 | 3.8 | μs |
| | | 15 | - | 0.9 | 2.9 | μs |
| | (2 ¹⁶) t _{PHL} , t _{PLH} | 5 | - | 6.0 | 18 | μs |
| | | 10 | - | 3.5 | 10 | μs |
| | | 15 | - | 2.5 | 7.5 | μs |
| Transition Time | t _{THL} | 5 | - | 100 | 200 | ns |
| | | 10 | - | 50 | 100 | ns |
| | | 15 | - | 40 | 80 | ns |
| | t _{THL} | 5 | - | 180 | 360 | ns |
| | | 10 | - | 90 | 180 | ns |
| | | 15 | - | 65 | 130 | ns |
| MASTER RESET, CLOCK Pulse Width | | 5 | 900 | 300 | - | ns |
| | | 10 | 300 | 100 | - | ns |
| | | 15 | 225 | 85 | - | ns |
| Maximum Clock Pulse Input Frequency | f _{CL} | 5 | - | 1.5 | - | MHz |
| | | 10 | - | 4 | - | MHz |
| | | 15 | - | 6 | - | MHz |
| Maximum Clock Pulse Input Rise or Fall time | t _r , t _f | 5, 10, 15 | Unlimited | | | μs |

Digital Timer Application

A positive pulse on MASTER RESET resets the counters and latch. The output goes high and remains high until the number of pulses, selected by A and B, are counted. This circuit is retriggerable and is as accurate as the input frequency. If additional accuracy is desired, an external clock can be used on pin 3. A setup time equal to the width of the one-shot output is required immediately following initial power up, during which time the output will be high.

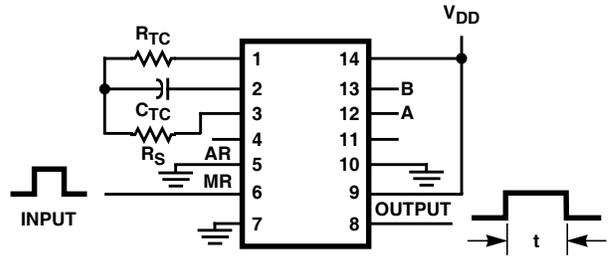


FIGURE 3. DIGITAL TIMER APPLICATION CIRCUIT

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| CD4541BE | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| CD4541BEE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| CD4541BF | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | |
| CD4541BF3A | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | |
| CD4541BM | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4541BM96 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4541BM96E4 | ACTIVE | SOIC | D | 14 | | TBD | Call TI | Call TI | |
| CD4541BM96G4 | ACTIVE | SOIC | D | 14 | | TBD | Call TI | Call TI | |
| CD4541BME4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4541BMG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4541BMT | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4541BMTE4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4541BMTG4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4541BNSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4541BNSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4541BNSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4541BPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4541BPWE4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4541BPWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| CD4541BPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4541BPWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4541BPWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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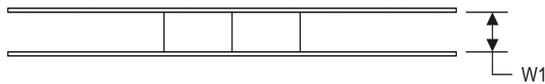
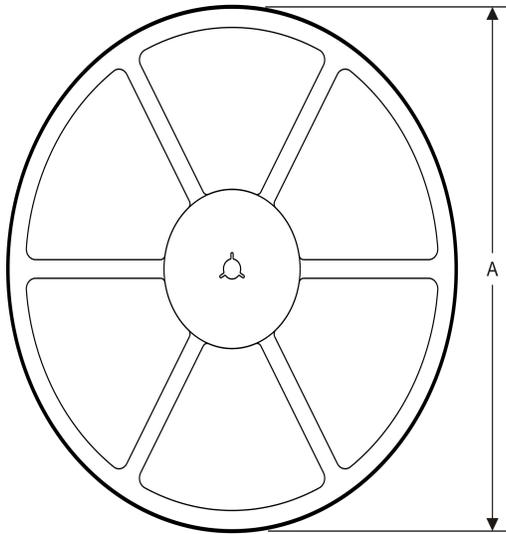
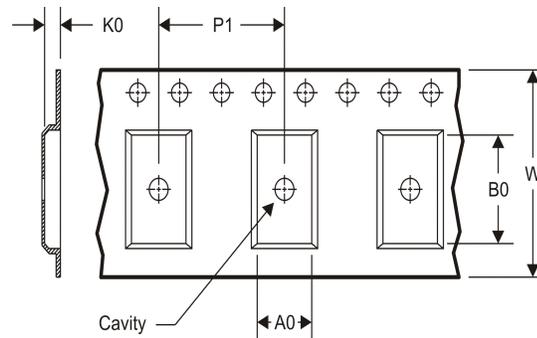
OTHER QUALIFIED VERSIONS OF CD4541B, CD4541B-MIL :

● Catalog: [CD4541B](#)

● Military: [CD4541B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4541BM96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4541BMT | SOIC | D | 14 | 250 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4541BNSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD4541BPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



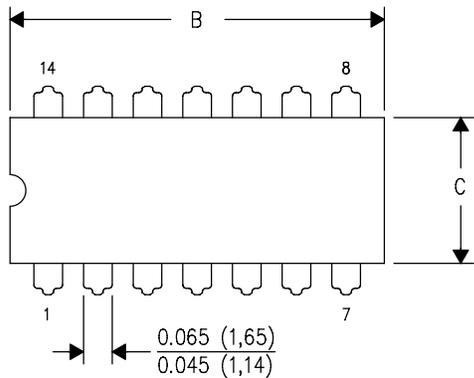
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4541BM96 | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| CD4541BMT | SOIC | D | 14 | 250 | 367.0 | 367.0 | 38.0 |
| CD4541BNSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| CD4541BPWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

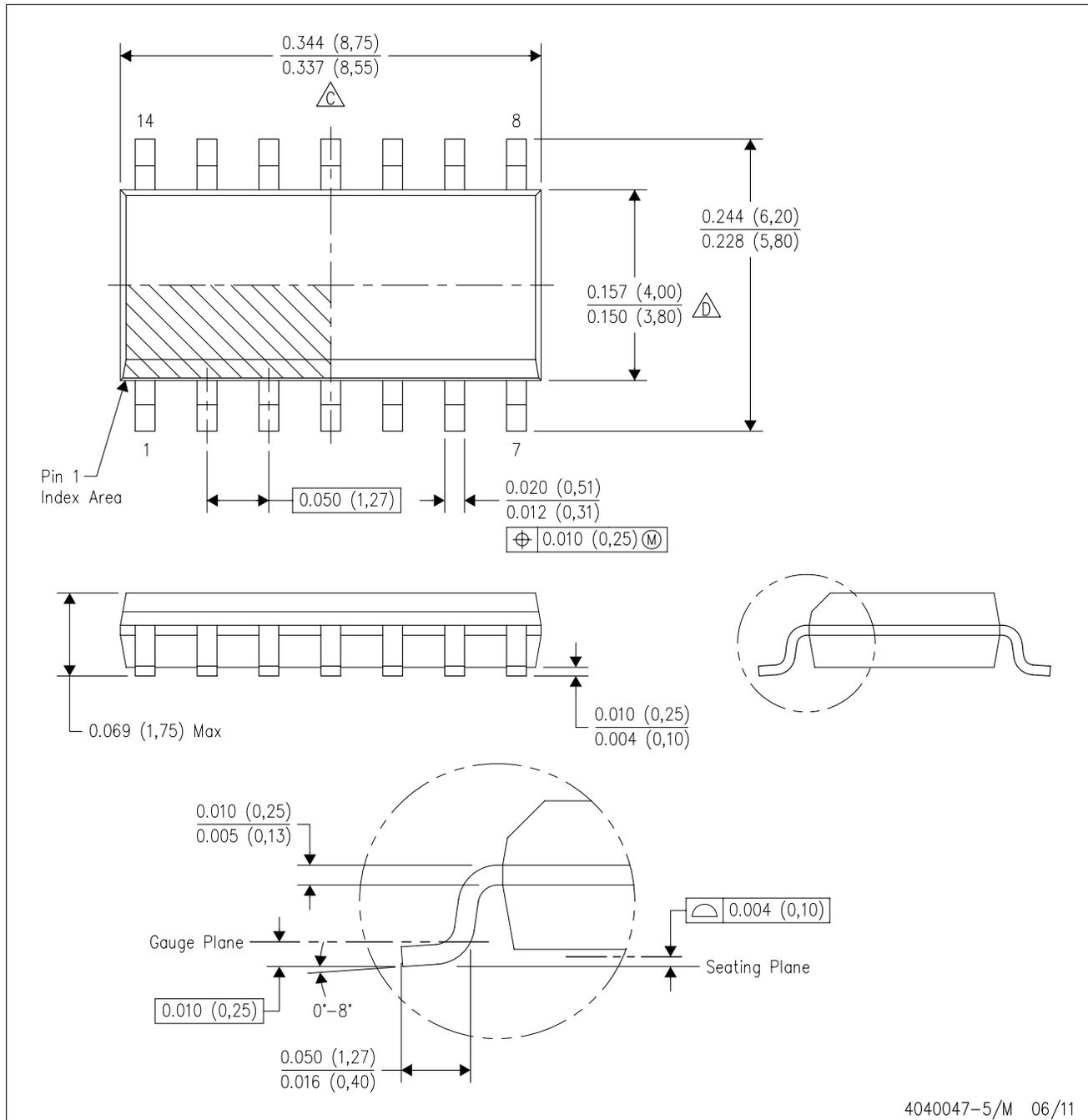


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- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

D (R-PDSO-G14)

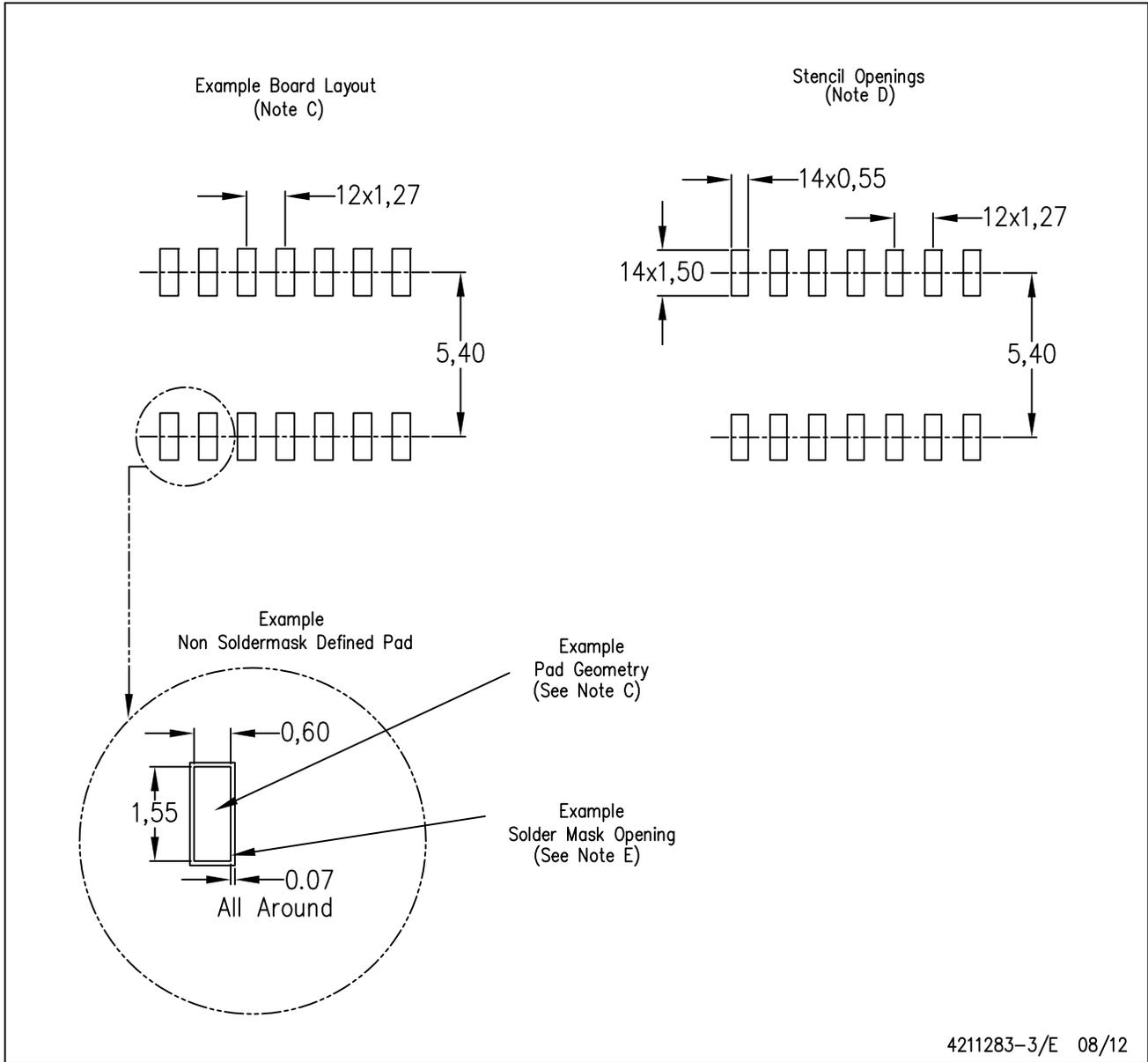
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

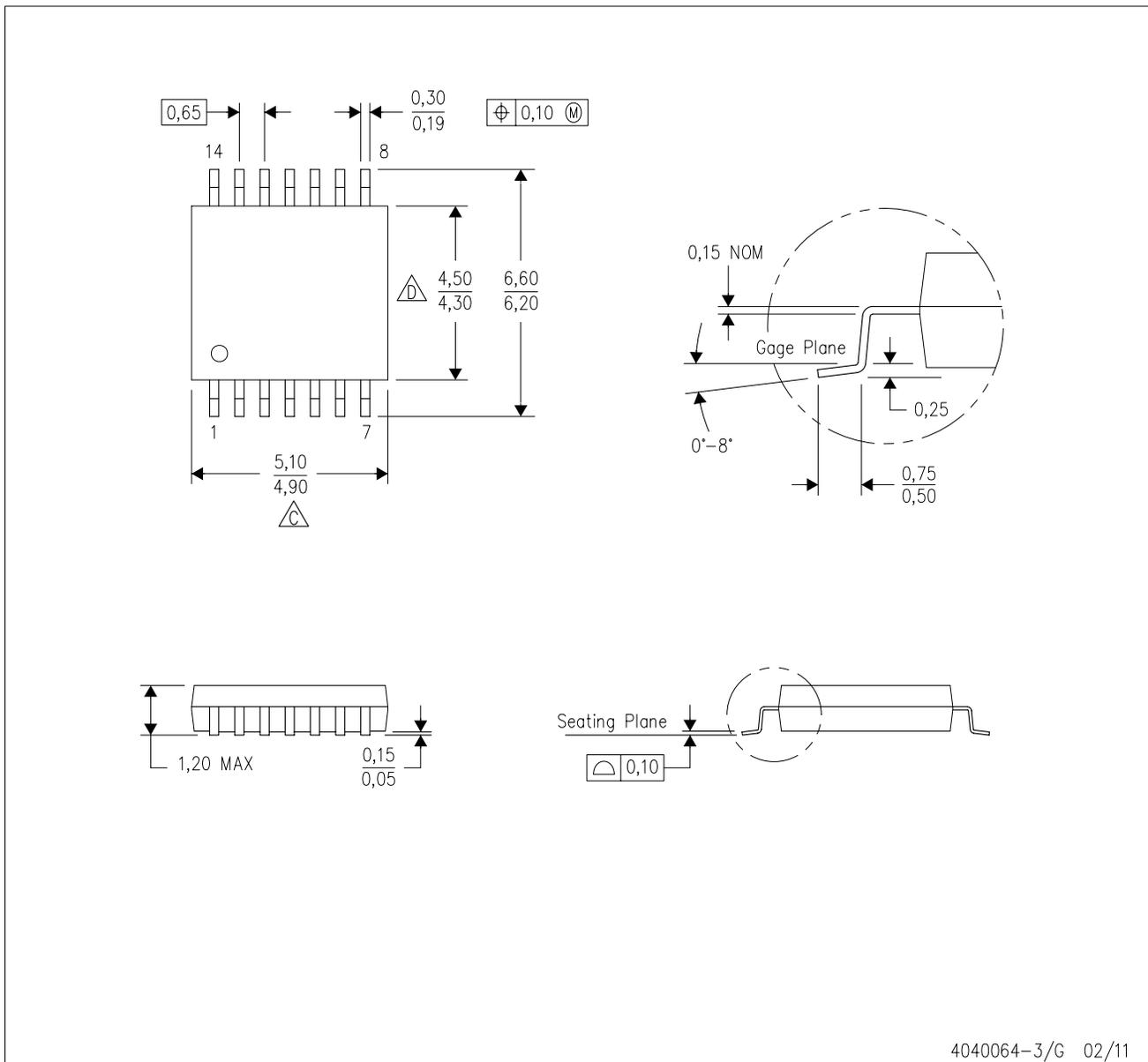
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

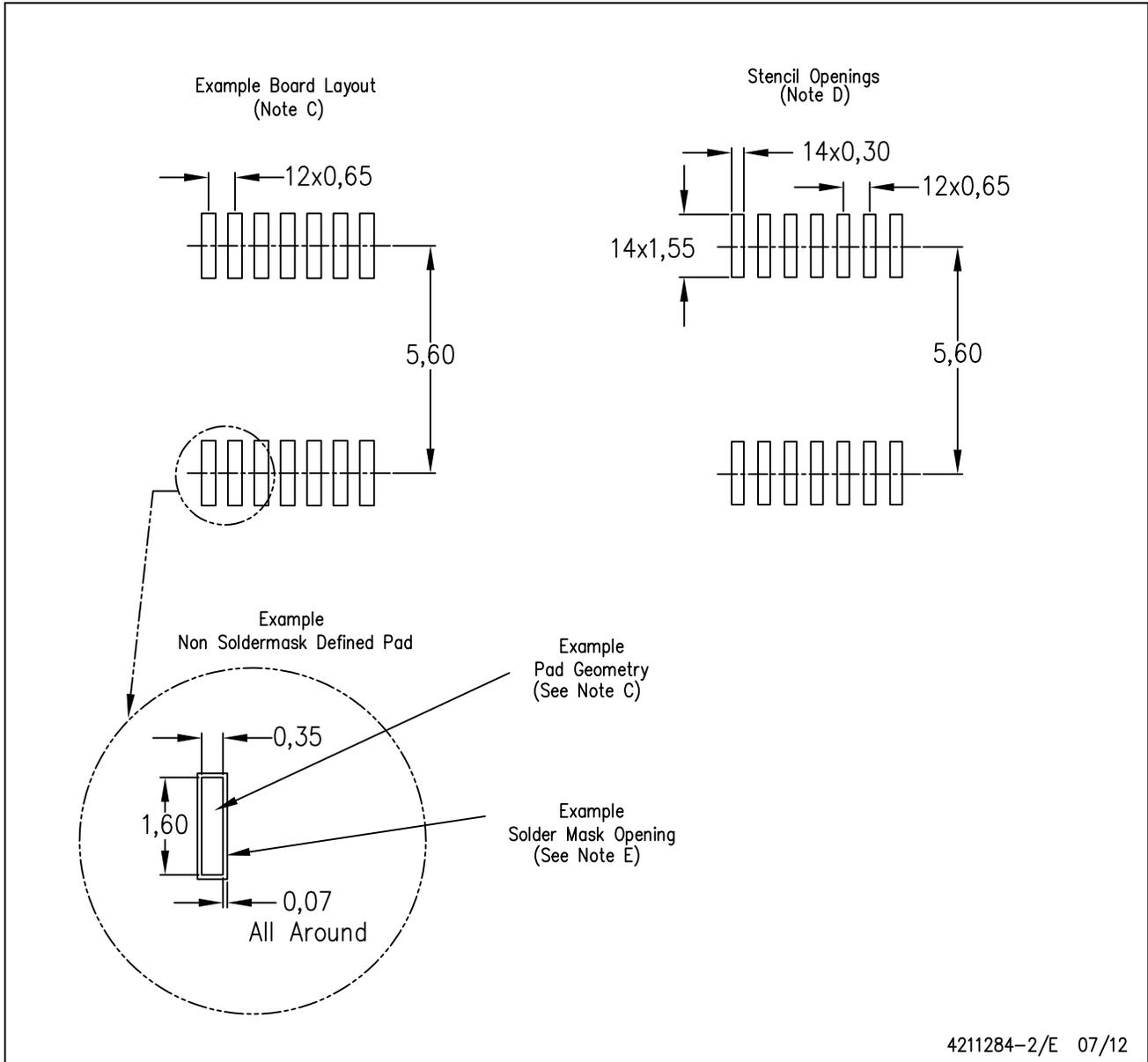
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



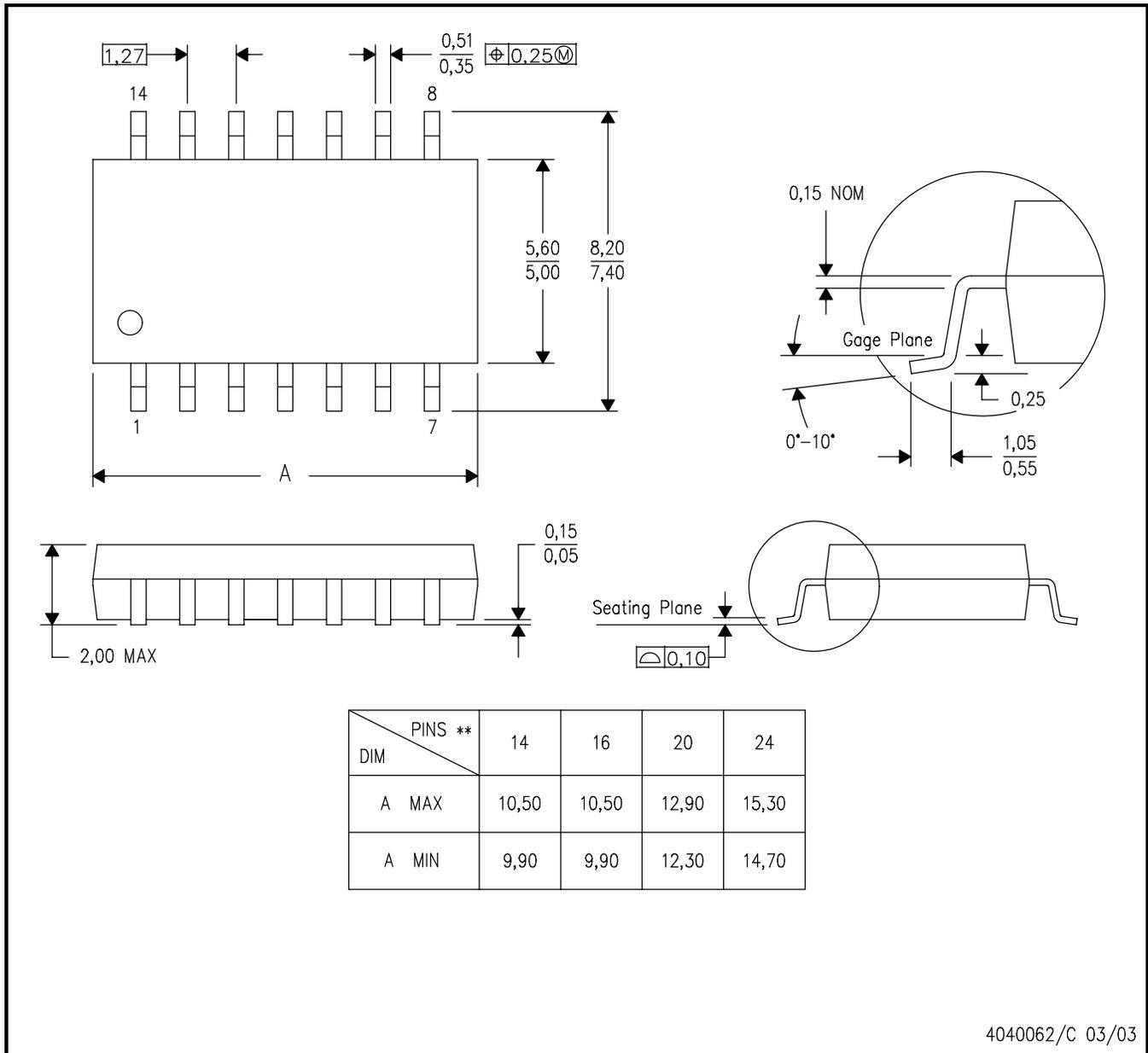
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

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