Panasonic

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DOCUMENT COVER PAGE

APPROVED

Note: This cover page establishes the Doc No., Title and current status of the attached gocurrent.

Doc No.	SDSC-PSE-AN7135	Issue Level	Rev	Eff Date
	3D3C-F3E-AN/133	1	5	23-FEB-06
Doc Title	Product Specifications for AN7135	Total no. of pag (excluding this	·	7

Revision History

Issue	Rev	Eff Date	S/N	Page	Change Details	Remarks
1	4	15-FEB-04	1	-	Added this cover page.	
			2	6	Removed this page.	
			3	6A	Added this page for leadfree specification.	
			4	6A	Amended Outer Lead Surface Process &	
					Chip Mounting Method.	
	5	23-FEB-06	1	6A	Amended Outer Lead Surface process.	
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Prepared Came	Product Specifications	EXTERNAL	ISSUE	
Checked And Wat	A NT7125	Totai Page	7	
Approved Board	AN7135	Page No.	1	

Structure	Silicon Monolithic Bipolar IC	
Appearance	FP12S Pin Plastic Package (with Fin)	
Application	Low Frequency Power Amplifier	
Function	7.5W(3Ω) x 2 Channel Power amplifier With Standby Function	

Α	Absolute Maximum Ratings							
No.	Item	Symbol Ratings Unit N						
1	Storage Temperature	Tstg	-55 ~ +150	° C	1			
2	Operating Ambient Temperature	Topr	-30 ~ +75	° C	1			
3	Operating Ambient Pressure	Popr	1.013x10 ⁵ ±0.61x10 ⁵	Pa				
4	Operating Constant Acceleration	Gopr	9,810	m/s²				
5	Operating Shock	Sopr	4,900	m/s ²				
6	Supply Voltage	Vcc	24	V				
7	Supply Current	ICC	4.0	A	- 			
8	Power Dissipation	PD	62.5	W	2			

Operating Supply Voltage Range	Vcc	$5V \sim 18V$	Note 3	ļ

Note 1: The temperature of all item shall be Ta=25°C except storage temperature and operating ambient temperature.

Note 2: $R_{\theta j-c} = 2.0^{\circ}C/W$

Note 3: 24V during no signal.

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B Electrical Characteristics (Unless otherwise specified, the ambient temperature is $25^{\circ}C \pm 2^{\circ}C$)									
No.	Item	Symbol	Test Cir-	Conditions		Limits		Unit	Note
110.		Symbol	cuit		min	typ	max		INOLE
1	Quiescent Circuit Current	Ιϲϙ	1	V _{IN} =0mV	æ	14	20	mA	
2	Output Noise Voltage	Vno	1	Vin=0mV, Rg=10kΩ	-	0.25	0.50	mV	1
3	Voltage Gain	Gv	1	V _{IN} =3mV	42.5	44.5	46.5	dB	
4	Total Harmonic Distortion	THD	1	V _{IN} =3mV		0.40	0.75	%	
5	Maximum Power Output	Ро	1	THD=10%	7.0	7.5		W	
6	Channel Balance	СВ	1	V _{IN} =3mV	-1	0	+1	dB	
7	Ripple Rejection	RR	1	Vcc(ripple) = 280mV f(ripple) = 120Hz Rg = 0 Ω Sine wave	45	50	-	dB	1
8	Input Offset Voltage	VIN (O.S)	1	Input pin open	-	10	30	mV	
9	Standy-by current	Іѕтв	1	Pin 3 open	-	H	30	μA	

< Vcc = 15.0V, RL = 3 Ω , Freq = 1kHz, Driving 2 channel >

Note 1) Use filter $15Hz \sim 30kHz$ (12dB/OCT) when measurement.

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Pin Descriptions

Pin No.	Description	Pin No.	Description
1	Channel 1 negative feedback	7	Channel 2 output
2	2 Channel 1 input		Channel 2 bootstrap
3	Repple filter / Stand-by	9	GND (Output side)
4	GND (Input side)	10	Power supply
5	Channel 2 input	11	Channel 1 bootstrap
6	Channel 2 negative feedback	12	Channel 1 output

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Prepared Checked	Yiap Shi Hui John Ng	Prod	uct Specifications (Leadfree)		RARPROVED EXotaEPANAL IS			
Approved	T. Sugimura		AN7135		Page No.	6A		
(Structure Description)								
Chip surfa	ace passivation	SiN,	PSG,	Othe	rs ()	1		
Lead fram	ne material	Fe group,	Cu group,	Othe	rs ()	(2), (6)		

Au plating,

Solder Plating (98Sn-2Bi)

Solder Dip (95.5Sn-2Ag-2Bi-0.5Cu)

Chip mounting method	Ag paste, Au-Si alloy, Solder (9	5.5Pb-2.5Ag-2S	5n)**,
Wire bonding method	Thermalsonic bonding,	Others ()
Wire material	Au,	Others ()
Mold material	(Epoxy,)	Others ()
Molding method	Transfer mold, Multiplunger mold,	Others ()
Fin material	Cu group,	Others ()

Ag plating,

SC Buyback:

General Customer:

Package FP12S

Inner lead surface process

Outer lead surface process

** Under RoHS exemption clause, Lead (Pb) in high melting temperature type solder (ie. tin-lead solder alloy containing more than 85% of lead), is exempted until 2010.

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Others (

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