4-TO-16 LINE DECODER/DEMULTIPLEXER WITH INPUT LATCHES; INVERTING

FEATURES

- **Inverting outputs**
- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT4515 are high-speed Si-gate CMOS devices and are pin compatible with "4515" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4515 are 4-to-16 line decoders/demultiplexers having four binary weighted address inputs (A_0 to A_3) with latches, a latch enable input ($\overline{LE}$), and an active LOW enable input ($\overline{E}$). The 16 inverting outputs ($\overline{O}_0$ to $\overline{O}_{15}$) are mutually exclusive active LOW. When LE is HIGH, the selected output is determined by the data on A_n. When LE goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When $\overline{E}$ is LOW, the selected output, determined by the contents of the latch, is LOW. When $\overline{E}$ is HIGH, all outputs are HIGH. The enable input ($\overline{E}$) does not affect the state of the latch.

When the "4515" is used as a demultiplexer, $\overline{E}$ is the data input and A_0 to A_3 are the address inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{O}_n$	C_L = 15 pF; V_{CC} = 5 V	25	26	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	44	46	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

24-lead DIL; plastic (SOT101A).
24-lead mini-pack; plastic (SO24; SOT137A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LE	latch enable input (active HIGH)
2, 3, 21, 22	A_0 to A_3	address inputs
11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	$\overline{O}_0$ to $\overline{O}_{15}$	multiplexer outputs (active LOW)
12	GND	ground (0 V)
23	$\overline{E}$	enable input (active LOW)
24	V_{CC}	positive supply voltage

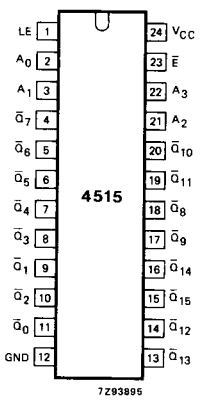

Fig. 1 Pin configuration.

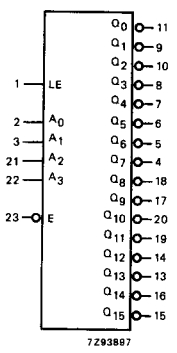

Fig. 2 Logic symbol.

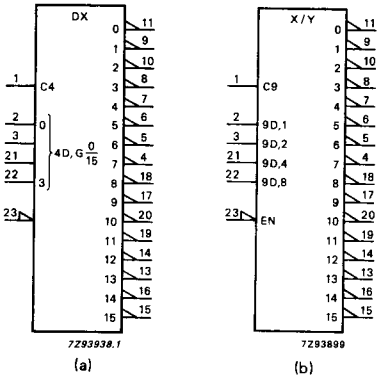

Fig. 3 IEC logic symbol.

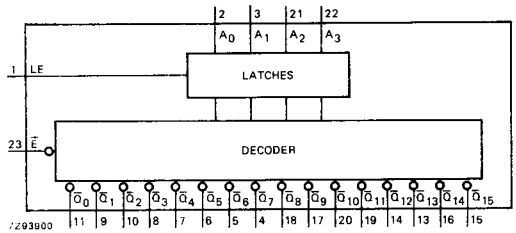

Fig. 4 Functional diagram.

APPLICATIONS

- **Digital mutliplexing**
- **Address decoding**
- **Hexadecimal/BCD decoding**

FUNCTION TABLE

INPUTS					OUTPUTS														
$\overline{E}$	A_0	A_1	A_2	A_3	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$	$\overline{O}_8$	$\overline{O}_9$	$\overline{O}_{10}$	$\overline{O}_{11}$	$\overline{O}_{12}$	$\overline{O}_{13}$	$\overline{O}_{14}$	$\overline{O}_{15}$
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

LE = HIGH
H = HIGH voltage level
L = LOW voltage level
X = don't care

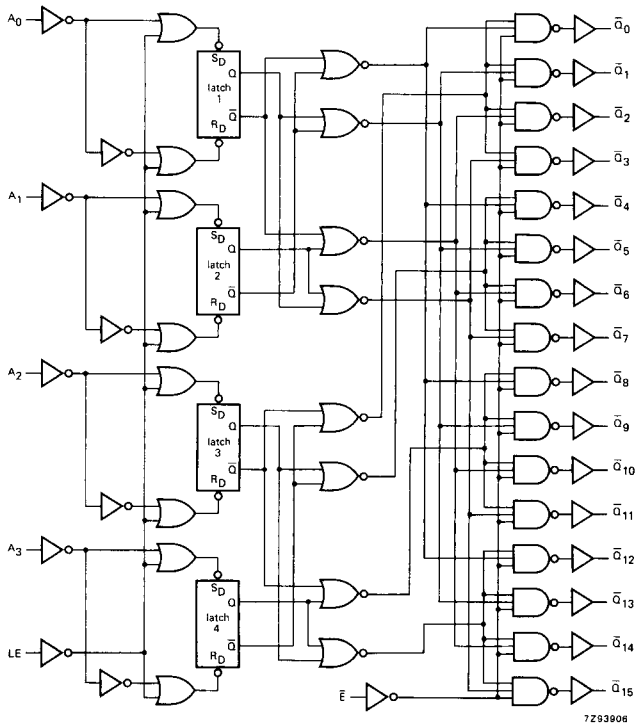

Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Q}_n$		80 29 23	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay LE to $\overline{Q}_n$		66 24 19	225 45 38		280 56 48		340 68 58	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to $\overline{Q}_n$		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	latch enable pulse width HIGH	75 15 13	14 5 4		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time A_n to LE	90 18 15	28 10 8		115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig. 7
t_h	hold time A_n to LE	0 0 0	−11 −4 −3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	0.65
LE	1.40
$\overline{E}$	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Q}_n$		30	55		69		83	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay LE to $\overline{Q}_n$		29	50		63		75	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to $\overline{Q}_n$		18	40		50		60	ns	4.5	Fig. 6
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	latch enable pulse width HIGH	16	3		20		24		ns	4.5	Fig. 7
t_{su}	set-up time A_n to LE	18	9		23		27		ns	4.5	Fig. 7
t_h	hold time A_n to LE	3	−2		3		3		ns	4.5	Fig. 7

AC WAVEFORMS

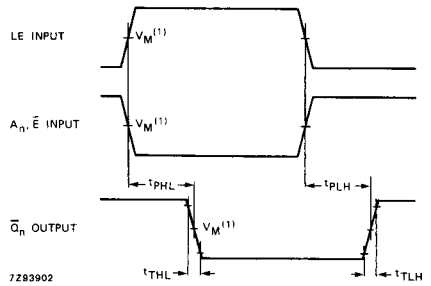

Fig. 6 Waveforms showing the input (A_n, LE, $\bar{E}$) to output ($\bar{Q}_n$) propagation delays and the output transition times.

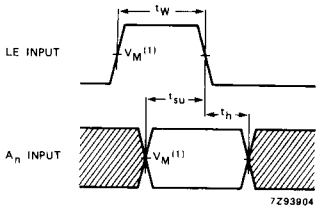

Fig. 7 Waveforms showing the minimum pulse width of the latch enable input (LE) and the set-up and hold times for LE to A_n. Set-up and hold times are shown as positive values but may be specified as negative values.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.