

25AA02E48

2K SPI Bus Serial EEPROM with EUI-48TM Node Identity

Device Selection Table

Part Number	Vcc Range	Page Size	Temp. Ranges	Packages
25AA02E48	1.8-5.5V	16 Bytes	I	SN, OT

Features:

- Pre-programmed Globally Unique, 48-bit Node Address
- Compatible with EUI-48[™] and EUI-64[™]
- 10 MHz max. Clock Frequency
- Low-Power CMOS Technology:
 - Max. Write Current: 5 mA at 5.5V
 - Read Current: 5 mA at 5.5V, 10 MHz
- Standby Current: 1 μA at 2.5V
- 256 x 8-bit Organization
- Write Page mode (up to 16 bytes)
- Sequential Read
- Self-Timed Erase and Write Cycles (5 ms max.)
- Block Write Protection:
 - Protect none, 1/4, 1/2 or all of array
- Built-in Write Protection:
 - Power-on/off data protection circuitry
 - Write enable latch
 - Write-protect pin
- High Reliability:
 - Endurance: 1,000,000 erase/write cycles
 - Data retention: >200 years
 - ESD protection: >4000V
- Temperature Ranges Supported:
 Industrial (I): -40°C to +85°C
- Pb-Free and RoHS Compliant

Pin Function Table

Name	Function			
CS	Chip Select Input			
SO	Serial Data Output			
WP	Write-Protect			
Vss	Ground			
SI	Serial Data Input			
SCK	Serial Clock Input			
HOLD	Hold Input			
Vcc	Supply Voltage			

Description:

The Microchip Technology Inc. 25AA02E48 is a 2 Kbit Serial Electrically Erasable Programmable Read-Only Memory (EEPROM). The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select (\overline{CS}) input.

Communication to the device can be paused via the hold pin (HOLD). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

The 25AA02E48 is available in the standard 8-lead SOIC and 6-lead SOT-23 packages.

Package Types (not to scale)

SOT-23 (OT)	SOIC (SN)	
SCK 료 1 6 원 Vpp Vss 료 ² 5 원 <u>CS</u> SI 료 ³ 4 원 SO	CS □ 8□ Vcc SO □ 7□ HOLD WP □ 6□ SCK Vss □ 4 5□	

Note: This document is supplemented by the "25AA020A Data Sheet" (DS21833). See Section 2.0 "Functional Description".

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings^(†)

Vcc	6.5V
All inputs and outputs w.r.t. Vss	-0.6V to Vcc +1.0V
Storage temperature	65°C to 150°C
Ambient temperature under bias	40°C to 85°C
ESD protection on all pins	4 kV

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

DC CHA	DC CHARACTERISTICS			TA =	-40°C to	+85°C Vcc = 1.8V to 5.5V
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Test Conditions
D001	VIH1	High-level Input voltage	0.7 Vcc	Vcc +1	V	
D002	VIL1	Low-level Input	-0.3	0.3 Vcc	V	Vcc ≥ 2.7V (Note 1)
D003	VIL2	Voltage	-0.3	0.2 Vcc	V	Vcc < 2.7V (Note 1)
D004	Vol	Low-level Output	—	0.4	V	IOL = 2.1 mA
D005	Vol	Voltage	—	0.2	V	IOL = 1.0 mA, VCC < 2.5V
D006	Voн	High-level Output Voltage	Vcc -0.5	—	V	ΙΟΗ = -400 μΑ
D007	ILI	Input Leakage Current	—	±1	μΑ	CS = Vcc, Vin = Vss to Vcc
D008	Ilo	Output Leakage Current	—	±1	μΑ	CS = Vcc, Vout = Vss to Vcc
D009	CINT	Internal Capacitance (all inputs and outputs)	—	7	pF	TA = 25°C, CLK = 1.0 MHz, Vcc = 5.0V (Note 1)
D010	ICC Read		—	5	mA	Vcc = 5.5V; FcLk = 10.0 MHz; SO = Open
		Operating Current	—	2.5	mA	Vcc = 2.5V; FcLк = 5.0 MHz; SO = Open
D011	Icc Write		—	5	mA	Vcc = 5.5V
			—	3	mA	Vcc = 2.5V
D012	Iccs	Standby Current	—	1	μΑ	\overline{CS} = Vcc = 2.5V, Inputs tied to Vcc or Vss, TA = +85°C

TABLE 1-1: DC CHARACTERISTICS

Note: This parameter is periodically sampled and not 100% tested.

AC CHA	AC CHARACTERISTICS			TA	= -40°C 1	to +85°C Vcc = 1.8V to 5.5V
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Test Conditions
1	FCLK	Clock Frequency		10 5 3	MHz MHz MHz	$\begin{array}{l} 4.5V \leq VCC < 5.5V \\ 2.5V \leq VCC < 4.5V \\ 1.8V \leq VCC < 2.5V \end{array}$
2	Tcss	CS Setup Time	50 100 150		ns ns ns	$4.5V \le VCC < 5.5V$ $2.5V \le VCC < 4.5V$ $1.8V \le VCC < 2.5V$
3	Тсѕн	CS Hold Time	100 200 250		ns ns ns	$4.5V \le VCC < 5.5V$ $2.5V \le VCC < 4.5V$ $1.8V \le VCC < 2.5V$
4	TCSD	CS Disable Time	50	_	ns	—
5	Tsu	Data Setup Time	10 20 30		ns ns ns	$4.5V \le VCC < 5.5V$ $2.5V \le VCC < 4.5V$ $1.8V \le VCC < 2.5V$
6	Тно	Data Hold Time	20 40 50		ns ns ns	$4.5V \le VCC < 5.5V$ $2.5V \le VCC < 4.5V$ $1.8V \le VCC < 2.5V$
7	TR	CLK Rise Time	—	100	ns	(Note 1)
8	TF	CLK Fall Time	_	100	ns	(Note 1)
9	Тні	Clock High Time	50 100 150		ns ns ns	$4.5V \le VCC < 5.5V$ $2.5V \le VCC < 4.5V$ $1.8V \le VCC < 2.5V$
10	Tlo	Clock Low Time	50 100 150		ns ns ns	$4.5V \le VCC < 5.5V$ $2.5V \le VCC < 4.5V$ $1.8V \le VCC < 2.5V$
11	TCLD	Clock Delay Time	50	_	ns	—
12	TCLE	Clock Enable Time	50	—	ns	—
13	T∨	Output Valid from Clock Low		50 100 160	ns ns ns	$4.5V \le VCC < 5.5V$ $2.5V \le VCC < 4.5V$ $1.8V \le VCC < 2.5V$
14	Тно	Output Hold Time	0		ns	(Note 1)
15	TDIS	Output Disable Time		40 80 160	ns ns ns	4.5V ≤ VCC < 5.5V (Note 1) 2.5V ≤ VCC < 4.5V (Note 1) 1.8V ≤ VCC < 2.5V (Note 1)
16	THS	HOLD Setup Time	20 40 80		ns ns ns	$\begin{array}{l} 4.5V \leq VCC < 5.5V \\ 2.5V \leq VCC < 4.5V \\ 1.8V \leq VCC < 2.5V \end{array}$

Note 1: This parameter is periodically sampled and not 100% tested.

- 2: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance[™] Model which can be obtained from Microchip's web site at www.Microchip.com.
- **3:** Twc begins on the rising edge of \overline{CS} after a valid write sequence and ends when the internal write cycle is complete.

AC CHARACTERISTICS			Industrial (I)	: TA	= -40°C t	to +85°C VCC = 1.8V to 5.5V
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Test Conditions
17	Тнн	HOLD Hold Time	20 40 80		ns ns ns	$4.5V \le Vcc < 5.5V$ $2.5V \le Vcc < 4.5V$ $1.8V \le Vcc < 2.5V$
18	THZ	HOLD Low to Output High-Z	30 60 160		ns ns ns	4.5V ≤ Vcc < 5.5V (Note 1) 2.5V ≤ Vcc < 4.5V (Note 1) 1.8V ≤ Vcc < 2.5V (Note 1)
19	Тн∨	HOLD High to Output Valid	30 60 160		ns ns ns	4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V
20	Twc	Internal Write Cycle Time (byte or page)	—	5	ms	(Note 3)
21	_	Endurance	1M	_	E/W Cycles	(Nоте 2)

TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

Note 1: This parameter is periodically sampled and not 100% tested.

- 2: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance[™] Model which can be obtained from Microchip's web site at www.Microchip.com.
- **3:** Twc begins on the rising edge of \overline{CS} after a valid write sequence and ends when the internal write cycle is complete.

TABLE 1-3:AC TEST CONDITIONS

AC Waveform:					
VLO = 0.2V	—				
VHI = VCC - 0.2V	(Note 1)				
VHI = 4.0V	(Note 2)				
CL = 100 pF	—				
Timing Measurement Reference Level					
Input	0.5 Vcc				
Output	0.5 Vcc				

Note 1: For VCC $\leq 4.0V$

2: For VCC > 4.0V

FIGURE 1-1: HOLD TIMING



FIGURE 1-2: SERIAL INPUT TIMING



FIGURE 1-3: SERIAL OUTPUT TIMING



2.0 FUNCTIONAL DESCRIPTION

2.1 **Principles of Operation**

The 25AA02E48 is a 256-byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC[®] microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in software to match the SPI protocol.

BLOCK DIAGRAM



Note: This data sheet documents only the device's features and specifications that are in addition to the features and specifications of the 25AA020A device. For information on the features and specifications shared by the 25AA02E48 and 25AA020A devices, see the "25AA020A Data Sheet" (DS21833).

3.0 PRE-PROGRAMMED EUI-48[™] NODE ADDRESS

The 25AA02E48 is programmed at the factory with a globally unique, EUI-48TM and EUI-64TM compatible node address stored in the upper 1/4 of the array and write-protected through the STATUS register. The remaining 1,536 bits are available for application use.



The 6-byte EUI-48[™] node address value is stored in array locations 0xFA through 0xFF, as shown in Figure 3-2. The first 3 bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority. The remaining 3 bytes are the Extension Identifier, and are generated by Microchip to ensure a globally-unique, 48-bit value.

3.1 EUI-64[™] Support

The pre-programmed EUI-48 node address can easily be encapsulated at the application level to form a globally unique, 64-bit node address for systems utilizing the EUI-64 standard. This is done by adding 0xFFFE between the OUI and the Extension Identifier, as shown below.





3.2 Factory-Programmed Write Protection

In order to help guard against accidental corruption of the EUI-48 node address, the BP1 and BP0 bits of the STATUS register are programmed at the factory to '0' and '1', respectively, as shown in the following table:

7	6	5	4	3	2	1	0
Х	Х	Х	Х	BP1	BP0	WEL	WIP
		_		0	1		—

This protects the upper 1/4 of the array (0xC0 to 0xFF) from write operations. This array block can be utilized for writing by clearing the BP bits with a Write Status Register (WRSR) instruction. Note that if this is performed, care must be taken to prevent overwriting the EUI-48 value.

4.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 4-1.

Name	SOIC	SOT-23	Function
CS	1	5	Chip Select Input
SO	2	4	Serial Data Output
WP	3	—	Write-Protect Pin
Vss	4	2	Ground
SI	5	3	Serial Data Input
SCK	6	1	Serial Clock Input
HOLD	7	—	Hold Input
Vcc	8	6	Supply Voltage

TABLE 4-1:	PIN FUNCTION TABLE

4.1 Chip Select (CS)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the \overline{CS} input signal. If \overline{CS} is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on \overline{CS} after a valid write sequence initiates an internal write cycle. After power-up, a low level on \overline{CS} is required prior to any sequence being initiated.

4.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25AA02E48. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

4.3 Write-Protect (WP)

The \overline{WP} pin is a hardware write-protect input pin. When it is low, all writes to the array or STATUS register are disabled, but any other operations function normally. When \overline{WP} is high, all functions, including nonvolatile writes operate normally. At any time, when \overline{WP} is low, the write enable Reset latch will be reset and programming will be inhibited. However, if a write cycle is already in progress, \overline{WP} going low will not change or disable the write cycle. See Table 2-4 for the Write-Protect Functionality Matrix.

4.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

4.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25AA02E48. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

4.6 Hold (HOLD)

The HOLD pin is used to suspend transmission to the 25AA02E48 while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the HOLD pin may be pulled low to pause further serial communication without resetting the serial sequence. The HOLD pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-tolow transition. The 25AA02E48 must remain selected during this sequence. The SI, SCK and SO pins are in a high-impedance state during the time the device is paused and transitions on these pins will be ignored. To resume serial communication, HOLD must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the HOLD line at any time will tri-state the SO line.

5.0 PACKAGING INFORMATION

5.1 Package Marking Information









Example:



	1st Line Marking Code			
Part Number	SOT-23			
	l Temp.			
25AA02E48	20NN			

Note: NN = Alphanumeric traceability code

Legend:	XXX	Part number or part number code				
	Т	Temperature (I, E)				
	Y	Year code (last digit of calendar year)				
	ΥY	Year code (last 2 digits of calendar year)				
	WW	Week code (week of January 1 is week '01')				
	NNN	Alphanumeric traceability code (2 characters for small packages)				
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)				
	\bigcirc					
Note:	Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.					
	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.					

Note: Please visit www.microchip.com/Pbfree for the latest information on Pb-free conversion.

*Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX	
Number of Pins	N	8			
Pitch	e		1.27 BSC		
Overall Height	A	-	-	1.75	
Molded Package Thickness	A2	1.25	-	_	
Standoff §	A1	0.10	-	0.25	
Overall Width	E	6.00 BSC			
Molded Package Width	E1	3.90 BSC			
Overall Length	D	4.90 BSC			
Chamfer (optional)	h	0.25	-	0.50	
Foot Length	L	0.40	-	1.27	
Footprint	L1	1.04 REF			
Foot Angle	φ	0°	-	8°	
Lead Thickness	С	0.17	-	0.25	
Lead Width	b	0.31	-	0.51	
Mold Draft Angle Top	α	5°	-	15°	
Mold Draft Angle Bottom	β	5°	_	15°	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.

- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	С		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	6			
Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	А	0.90	_	1.45
Molded Package Thickness	A2	0.89	_	1.30
Standoff	A1	0.00	-	0.15
Overall Width	E	2.20	_	3.20
Molded Package Width	E1	1.30	_	1.80
Overall Length	D	2.70	-	3.10
Foot Length	L	0.10	_	0.60
Footprint	L1	0.35	_	0.80
Foot Angle	φ	0°	_	30°
Lead Thickness	С	0.08	_	0.26
Lead Width	b	0.20	_	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.

2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

APPENDIX A: REVISION HISTORY

Revision A (12/08)

Original release of this document.

25AA02E48

NOTES:

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_		
_		
6. Is	s there any incorrect or misleading in	nformation (what and where)?
_		
_		
7. ⊦	low would you improve this docume	nt?
_		
_		

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	×	- <u>x /xx</u>	Ex	kamples:
Device	Tape & Re	el Temperature Package	a)	25AA02E48-I/SN = 2k-bit, 16-byte page, 1.8V Serial EEPROM, Industrial temp., SOIC pack- age
Device:	25AA02E48	2k-Bit, 1.8V, 16 Byte Page, SPI Serial EEPROM with EUI-48™ Node Identity		25AA02E48T-I/SN = 2k-bit, 16-byte page, 1.8V Serial EEPROM, Industrial temp., Tape & Reel, SOIC package 25AA02E48T-I/OT = 2k-bit, 16-byte page, 1.8V
Tape & Reel:	Blank = T =	Standard packaging Tape & Reel	c)	Serial EEPROM, Industrial temp., Tape & Reel, SOT-23 package
Temperature Range:	I =	-40°C to+85°C		
Package:	SN = OT =	Plastic SOIC (3.90 mm body), 8-lead SOT-23, 6-lead (Tape and Reel only)		

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NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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