T- 7 S— 27-0 7

FSK Demodulator/Tone Decoder

GENERAL DESCRIPTION

TYB XR-2211 is a monolihic phase-locked loop (PLL) system especially &signed for data communications applications. It is particularly suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01 Hz to 300kHz. It can accommodate analog signals between 2mV and 3V, and can interface with conventional DTL, TTL, and ECL logié families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK vol* comparator which provides FSK demodulation. Extemal components are used to independently set center frequency, bandwidth, and output delay. An internal voltage reference proportional to the power supply provides raionometric operation for low system performance variations with power supply changes.

The XR-2211 is available in 14 pin DIP ceramic or plastic packages specified for commercial or military temperature ranges.

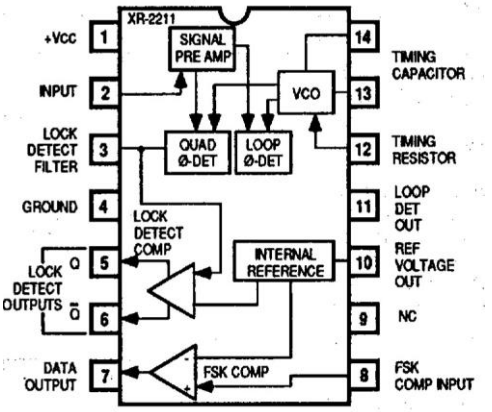
FEATURES

Wide Frequency Range 0.01 Hz to 300kHz
WWe Supply Voltage Range 4.5V to 20V
HCMOS/TTULogic Compatibility
FSK Demodulation, wit! Carrier Detection
Wide Dynamic Range 2mV to 3V rms
Adjustable Tracking Range (±1% to 80%)
Excellent Temp. Stability 20 ppmPC, typ.

APPUCATIONS

FSK Demodulaüon
Data Synchronization
Tone Decoding

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply 20V
Input Signal Level 3V rms Power Dissipaion 900mW Ceramic Package750mW

Derate Above TA = +25^{0}C 8mW/OC
Plastic Package 800mW
Derate Above TA = +25^{0}C 60mW/OC
JEDEC SO 390mW

ORDERING INFORMATION

Part Number Package Operating Temperature

XR-2211

FM Detection

Carrier Detection

XR-2211M	Ceramic	-55°C to +125°C
XR-2211CN	Ceramic	O° C to +70°C
XR-2211CP	Plastic	O°C to +70°C
XR-2211N	Ceramic	-4000 to +850C
XR-2211P	Plastic	to +85°C
XR-2211D	JEDEC SO-14	O°C to +70°C

Derate Above TA = +25°C5mWPC

ELECTRICAL CHARACTERISTICS

Test Conditions: 12V, TA = +25°C. Ro = 30KQ, co = O.033gF.

PARAMETER	21112211M MIN	21112211M TYP	21112211M MAX	XR-2211C MIN	XR-2211C TYP	XR-2211C MAX	UNITS	CONDITIONS
GENERAL								
Supply Voltage	4.5		20	4.5		20		
Supply Curreent		4	7		5	9	mA	10kQ. See Fig. 4
OSCILLATOR SECTION								
Frequency Accuracy		11	13		11			Deviation
Frequency Stabiliy								RI = 1/2 from fo 1/RoCo
Temperature					120			See Figure 8.
Power Supply		120	150		0.05		pprn/0C	IV. See Fig. 7.
		0.05	0.5		0.2			
Upper Frequenq Limit I-		0.2						5±0.5V. See Fig. 7.
Nest Practical	100	300						Ro 8.2kQ, CO 400*
Operaing Frequenq[t]					0.01		kHz	
Timing Resistor, Ro			0.01					Ro = 2MQ, CO 50pF See Fig. 5.
Operating Range								
Recommended Range 1	5		2000	5		2000		
	15			5		100	kQ	See Figs. 7 and 8.
LOOP PHASE DETECTOR SECTION								
Peak Output Current a:tput	1150	1200	1300	1	*200	±300		Measured at Pin 11.
				100	±21			
Offset Current					±5		PA	
Q.nput Impedance	14	1						Referenced to Pin 10.
Maximum Swing				14			V	

ADRATURE PHASE DETECTOR								Measured at Pin 3.
Peak Output Current OuVut Imped Maximum Swing	100 .	150 1 11			.1 11		V pp	
INPUT PREAMP SECTION								at Pin 2.
Input Impedance Input Signal Voltage Required Cause Limiting	.				.		rms	
VOLTAGE COMPARATOR SECTION								
Input Impedance Input Bias Current Voltage Gain Output Voltage Low a- ltput Leakage Current	55	2 100 70 0.01			2 100 55 70 0.01		nA dB	Measured at Pins 3 and 8. RL-5.1kn 3mA vo=20V
INTERNAL REFERENCE								
Voltage Level a- ltput Impedance Maximum Source Current	4.9 .	5.3 100 80	5.7 .	4.75	5.3 100 80	5.85 .	Q PA	Wasured at Pin 10. AC Small Signal

*These parameters, although guaranteed over the recommended operating condiions, are not 100% tested in producion.

SYSTEM DESCRIPTION

The output of he phase detector produces sum and difference frequencies of the input and the VCO (internally connected). When in lock, ttese frequendes are flN + fvco (2 times flN when in lock) and flN — fvco (OHZ when lock). By adding a capacitor to tie phase detector the 2 imes flN component is reduced, leaving a DC voltage that represents the phase difference between the two frequencies. This closes the loop and allows the VCO to track the input frequency.

The other sections of the XR-2211 act to: determine if the VCO is driven above or below the center frequency (FSK comparator); produced both active high and active low outputs to indicate when the main PLL is in lock (quadrature phase detector and lock detector comparator).

PRINCIPLES OF OPERATION

Signal Input (Pin 2): Signal is ac coupled to this terminal. The internal impedance at Pin 2 is 20KQ. Recommended input signal level is in the range of 10mV rms to 3V ms.

Quadrature Phase Detector Output (Pin 3): This is the high impedance output of quadrature phase detector and js intemally connected to tie input of lock detect voltage comparator. In tone detection applications, Pin 3 is

connected to ground through a parallel combination of RD and CD (see Figure 2) to eliminate the chatter at lock detect outputs. It the tone detect section is not used, Pin 3 can be left open circuited.

Lock Detect Output, Q (Pin 5): The output at Pin 5 is at 'high" state when the PLL is out of lock and goes to "low"or conducting state when he PLL is locked. It is an open collector type and requires a puil-up resistor, RL, to V+ for proper operation. At "low" state, it can sink up to 5mA of load current.

Lock Detect Complement, Q (Pin 6): The output at Pin 6 is he logic complement of fre lock detect output at Pin 5. This output is also an open collector type stage which can sink 5mA of load current at low or "on" state.

FSK Data Output (Pin 7): This output is an open collector logic stage which requires a pull-up resistor, R', to V+ for proper operation. It nn sink 5mA of load current. When decoding FSK signals, FSK data output is at "high" or "off" state for low input frequency, and at "bw" or "on* state for high input frequency. If no input signal is present, the logic state at Pin 7 is in&terminate,

FSK Comparator Input (Pin 8): This is the high impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase detector output (Pin 11). This data filter is formed by RF and CF of Figure 2. The threshold voltage of the comparator is set by tie intemal reference voltage, VR, available at Pin 10.

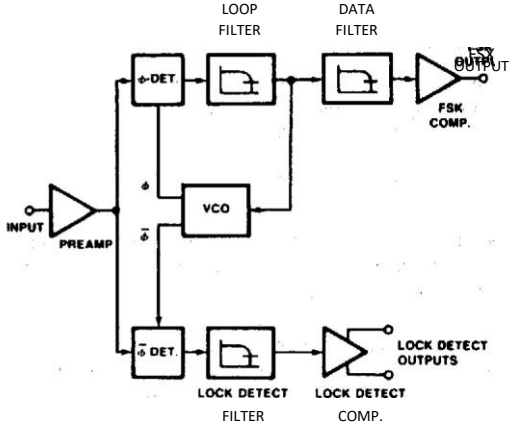


Figure 1. Functional Block Diagram of a Tone end FSK Decoding System Using XR-2211

Reference Voltage, VR (Pin 10): This pin is intemally biased at he reference voltage level, VA: VR = V + /2 — 650mV. The dc voltage level at this pin forms an intemal reference for the voltage levels at Pins 5, 8, 11 and 12. Pin 10 must be bypassed to ground with a O. 1 BF capacitor for proper operation of fre circuit.

Loop Phase Detector Output (Pin 11): This terminal provi±s a high impedance output for the loop phase detector. The PLL loop filter is formed by RI and Cl connected to Pin 11 (see Figure. 2). With no input signal, or with no phase error within the PLL, the dc level at Pin 11 is very nearly equal to VR. The peak voltage swing available at the phase etector is equal to ±VR.

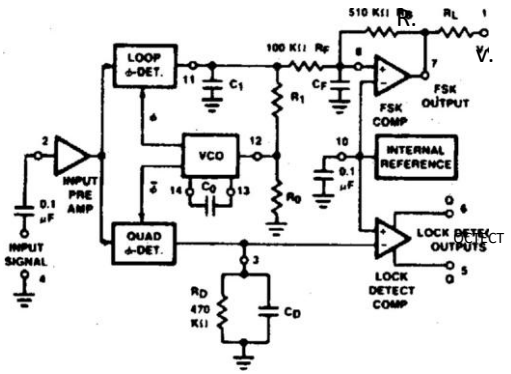


Figure 2. Gneralized Circuit Connection for FSK and Tone Detection

VCO Control Input (Pin 12): VCO free-running

frequency is determined by extemal timing resistor, Ror connected from this terminal to ground. The VCO freetunning frequency, fo, is:

$$\frac{1}{R_O C_O} \text{ Hz}$$

where Co is the timing capacitor across Pins 13 and 14. For optimum temperature stabiliy, Ro must be in the ranp of 10KQ to 100KQ see FWre 8).

This terminal is a low impedance point, and is internally

biased at a dc level equal to VA. Tt•e maximum timing curra't drawn from Pin 12 must be limited to s 3mA for proper opera60n of he circuit.

VCO Tlming Capacitor (Pins 13 and 14): VCO

frequency is inversely proportional to the external

iming capacitor, Co, connected across these terminals (see Figure 5). Co must be nonpolar, and in the range

at known mark and space frequencies. By adjusting the VCO can hen be Wned to obtain a 50% duty cycle on he FSK output (pin 7). This wil ensure that the VCO fo value is accurately referenced to tie mark and space frequer•Os.

DESIGN EQUATIONS

(See Figure 2 for definiton of components.)

I. VCO Center Frequency, fo: $f_0 = 1/R_O C_O$ Hz

2. Internal Reference Voltage, VR (rneasured at Pin 10):

V_R = V+/2 650mV

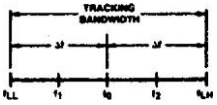
3. Loop Low-Pass Filter Time Constant, t:

$\tau = R_I C_I$

4. Loop Damping. G:

5. Loop Tracking Bandwidth, ±åf/fo:

$\Delta f/f_0 = R_O/R_I$



6. FSK Data Filter Time Constant, CF:

$\tau_F = R_F C_F$

7. Loop Phase Detector Conversion Gain, Kø: (Kø is the differential dc voltage across Pins 10 and 1 1, per unit of phase error at phase detector input):

Kø = 02VR/1t volts/radian

of 200pF to IV.

VCO Frequency Adjustment: VCO can be fine-tuned by connecöng a potentiometer, Rx, in series witl Ro at Pin 12 (see Figure 9).

VCO Free-Running Frequency, fo: XR-2211 not have a separate VCO output terminal. Instead, the VCO outputs are internally cönnected to the phase detector sections of the circuit. For set-up or adjustment purposes, he VCO free-running frequency can be uned by using he generalized circuit in Figure 2, and applying an altemating bit pattern of o's and I's

8. VCO Conversion gain, Ko: (Ko is the amount of change in VCO frequency, per unit of dc voltage change at Pin 1 1):

   Ko = -INRCoRl Hz/volt

9. Total Loop Gain, KT:

   KT 21tKøKo 4/coRl rad/seuvolt

10. Peak Phase Detector Current IA:
    IA = (volts)/25mA

APPLICATIONS INFORMATION

FSK Decoding

Figure 9 shows the basic circuit connecüon for FSK decoding. With reference to Figures 2 and 9, the functions of external components are defined as follows: Ro and Co set be PLL center frequenq, RI sets the system bandNidth, and Cl sets he loop filter ime constant and tie loop damping factor. CF and RF form a one-pole post-detection filter for the FSK data output. The resistor RB (z 510KQ) from Pin 7 to Pin 8 introduces positive feedback across the FSK comparator to fadlitate rapid tansition beween output logic states. Recommended component values for some of the most commonly used FSK bands are given in Table 1.

Design Instructions:

The circuit of Figure 9 can be tailored for any FSK decoding applicaöon by the choice of five key circuit components: Ro, RI, Co, Cl and CF. For a given set of FSK mark and space frequencies, fl and f2, these parameters can be calculated as follows:

a) Calculate PLL center frequency, fo:

$$f_0 = \frac{f_1 + f_2}{2}$$

b) Choose value of timing resistor Ro, to be in the range of 10KQ to IOOKQ. This choice is arbitrary. The recommended value is Ro = 20KQ. The final value of Ro is normally fine-tuned with the series potentiometer, Rx.

c) Calculate value of Co from design equation (1) or from Figure 6:

   co = 1/R0f0

d) Calculate RI to give a Af equal to fre mark space deviation:

   $R_1 = R_0[f_0/(f_1 - f_2)]$

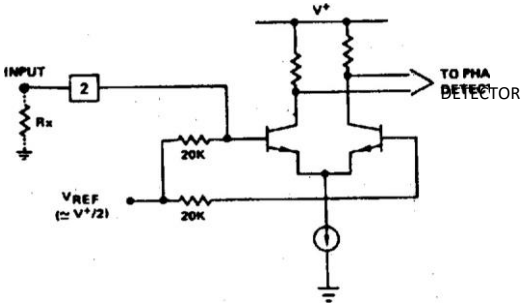
e) Calculate Cl to set loop damping. (See design equation No.4.):

   Normally, — 1/2 is recommen&d.

   Then: for 1/2

f) The input to the XR-221 1 may sometimes be to sensitive to noise conditions on the input line.

Figure 3 illustrates a meti0d of de-sensitizing the XR-2211 from such noisy line conditions by the use of a resistor, Rx, connected from pin 2 to ground. The value of Rx is chosen by the eqaation and frte desired minimum signal threshold level.



VIN (PEAR) V+ * 2.8 mV

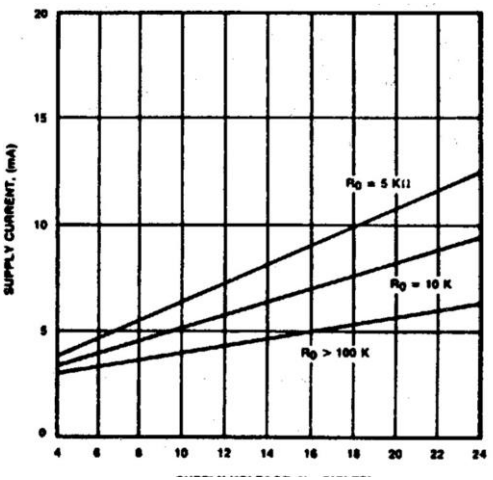
Figure 3. Desensitizing Input Stage

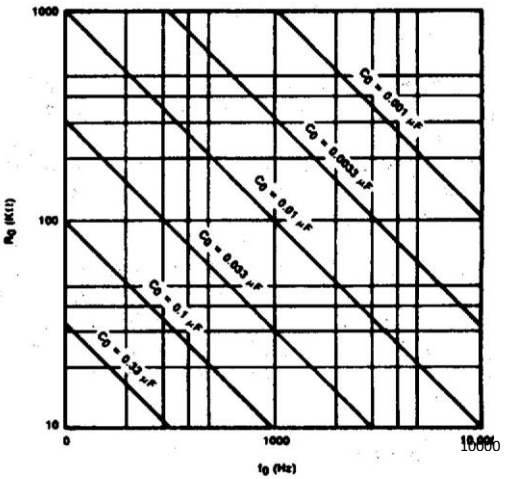
g) Calculate Data Filter Capacitance, CF:

For RF = IOOKQ, RB = 51 OKQ, the recommended value of CF is:

CF 3/(Baud Rate) PF

Note: All calculated component values except Ro can be roun&d to the nearest standard value, and Ro can be varied to fine-tune center frequency, through a series potentiometer, Rx. (See Figure 9.).





iiiiiihii

to 12

SUPRY VOLTAGE. V. (vocrs)

Flgure 4. Typical Supply Currentvs V+ (Logic OutputsOpenCircuited)

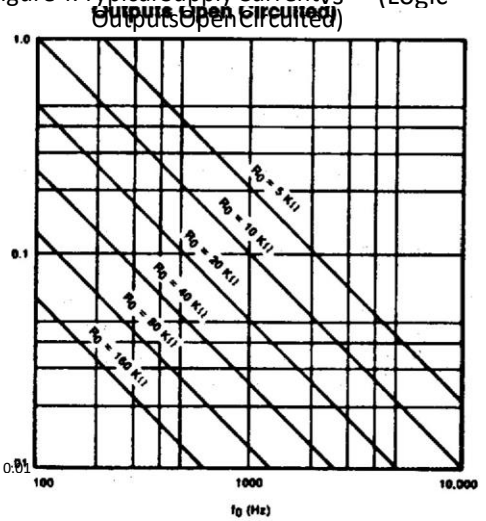


Figure 5. VCO Frequency vs Timing Resistor

Flgure 6. VCO Frequencyvs Timing Capacitor

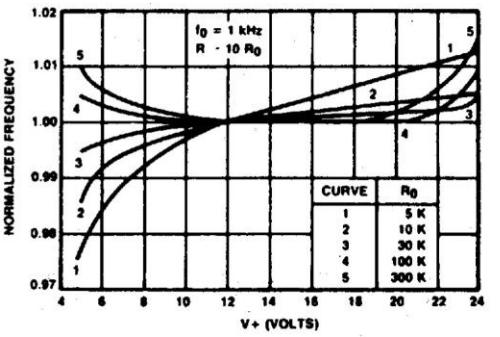
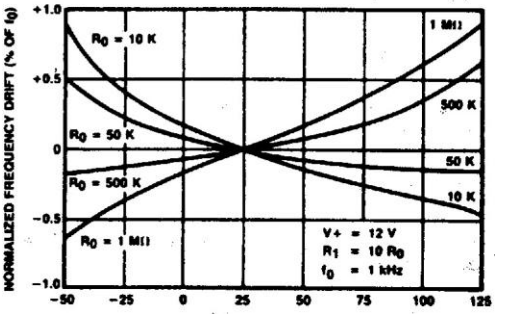


Figure 7. Typical f_0 vs Power Supply Characteristics



TEWERATURECC)

Figure 8. Typical Center FrequencyDrift vs u aa 24 V.

(VOLTS)

Figure 7. Typical fo vs Power Supply Characteristics

to (HE)

Temperature

D ■ 3422618ooossqo ⁱ-ISB —EXR

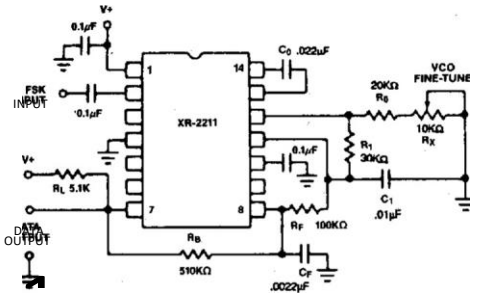


Figure 9. Circuit Connection for FSK Decoding of Caller Identification Signals (Bell 202 Format) Design Example:

1200 Baud FSK demodulator with mark space frequencies of 1200/2200Hz:

step 1: Calculate fo: fo (1200 + 2200) (1/2) = 1700Hz

Step 2: Choose Ro 26.7KQ (20KQ fixed resistor in series with 10KQ potentiometer)

Step 3: Calculate Co from design equation 1: yielding co = 0.022gF step 4: Calculate RI: RI = Ro (1700/1000) 45KQ

step 5: Calculate Cl: = $C_0/4 = 0.055\mu F \approx 0.01gf$

Note: All values except Ro can be rounded to nearest standard value.

Table 1. Recommended Component Values for Commonly Used FSK Bands. (See Circuit or Figure 10.)

300 Baud = 1070 Hz	co = 0.039gF
1270 Hz 300 Baud fl = 2025 Hz f2 = 2225 Hz Caller I.D. Rec'v (1200 Baud) 1 = 1200 Hz 2 = 2200 Hz	= O.01gF CF = O.005gF RI = Ro = 18KQ co = 0.022gF = 0 0047pF CF = 0 005gF RI = 200KQ Ro = 18KQ co = O.022pF Cl = 0.01gF RI 45KQ = O.0022pF RO = 26 7KQ CD =O.IPF 470KQ

FSK Decoding with Carrier Detect

The lock detect section of XR-2211 can be used as a carrier detect option, for FSK decoding. The recommended drcuit connection for this application is shown in Figure 10. The open collector lock detect output, Pin 6, is shorted to data output (Pin 7). Thus, data output will be disabled at "low" state, until there is a carrier within fre detection band of the PLL and the Pin 6 output goes "high," to enable the data output.

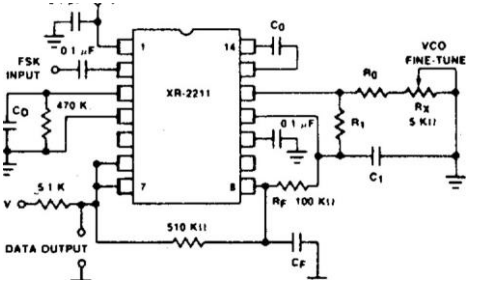


Figure 10. External Connectors for FSK Demodulation with Carrier Detect Capability

Note: Data Output is "Low" When No Carrier is Present.

The minimum value of the lock detect filter capacitance CD is inversely proportional to the capture range, ±Afc. This is the range of incoming frequencies over which tie loop can

acquire lock and is always less than the tracking range. It is further limited by Cl. For most applications, Afc > Af/2. For RD = 470KQ, the approximate minimum value of CD can be determined by:

CD (BF) 2 16/capture range in Hz.

With values of CD that are too small, chatter can be observed on the lock detect output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of CD will slow the response time of the lock detect output. For Caller I.D. applications choose CD = O. 1 BF.

Tone Detection

Figure 11 shows the generalized circuit connection for tone detection. The logic outputs. Q and Q at Pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs become reversed for the duration of tie input tone. Each logic output can sink 5mA of load current.

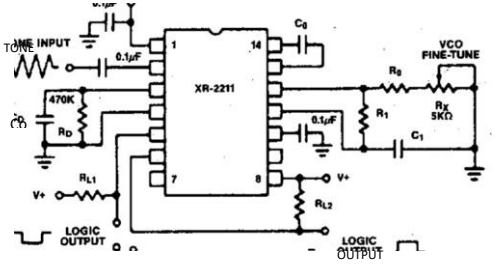


Figure 11. Circuit Connection for Tone Detection

Both logic outputs at Pins 5 and 6 are open collector type stages, and require extemal pull-up resistors RLI and RL2, as shown in Figure 11.

With reference to Figures 2 and I I, the funcöons of the external circuit components can be explained as follows: Ro and Co set VCO center frequency; RI sets the detection bandwidth; Cl sets the low pass-loop filter time constant and the loop damping factor. RLI and RL2 are fre respecfive pull-up resistors for the Q and Q logic outputs.

Design Instructions:

The circuit of Figure 11 can be optimized for any tone detection application by the choice of the 5 key circuit: components: Ro, RI, Co, Cl and CD. For a given input, the tone frequency, fs, these parameters are calculated as follows:

a) Choose Ro to be in he range of 15KQ to IOOKQ. This choice is arbitrary.

b) Calculate Co to set center frequency, fo equal to fs (see Figure 6): Co = 1/Rofs.

c) Calculate RI to set bandwidth (see design equation No. 5):

D 3422618 54 1 39 14 ZEXR

RI = Ro(fo/åf)

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Note: TYE étection bandwidh covers he frequency range of fo ± M.

d) Calculate value of Cl for a given loop damping factor;

Cl = co/16 G2

Normally 1/2 is optimum for most tone detector applications, giving Cl = 0.25 Co.

Increasing Cl improves the out-of-band signal rejection, but increases the PLL capture ime.

e) Calculate value of filter capacitor CD. To avoid chatter at the logic output, with RD = 470KQ, CD must be:

CD(PF) (16/capture range in Hz)

Increasing CD slows down the logic output response time.

Design Examples:

Tone detector with a étection band of 1kHz ± 20Hz:

a) Choose Ro = 20KQ (18KQ in series with 5KQ potentiometer).

b) Choose Co for fo = 1kHz (from Figure 6): Co = O.05gF.

c) Calculate RI : RI = (Ro) (1000/20) = IMO.

d) Calculate : for G 1/2, Cl = 0.25, co = 0.013gF

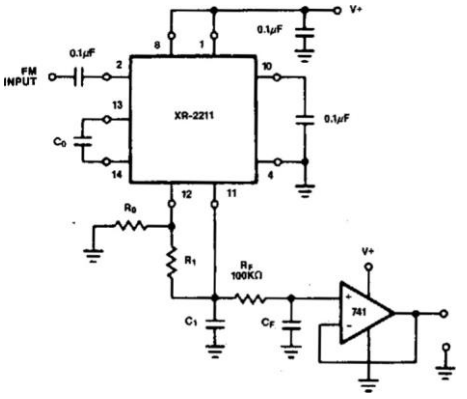
e) Calculate co: CD - 16/38 = 0.42pF. .

f) Fine-tune center frequency with 5KQ potenüometer,

Linear FM Detection

XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommen&d circuit connection for this application is shown in Figure 12. The demodulated output is taken from the loop phase étector output (Pin 1 1), through a postotection filter made up of RF and CF, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at Pin 11. Normally, a noninverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 12.

T-75-27-07 per unit of FM deviation can be given as:



DEMOD. OUTPUT

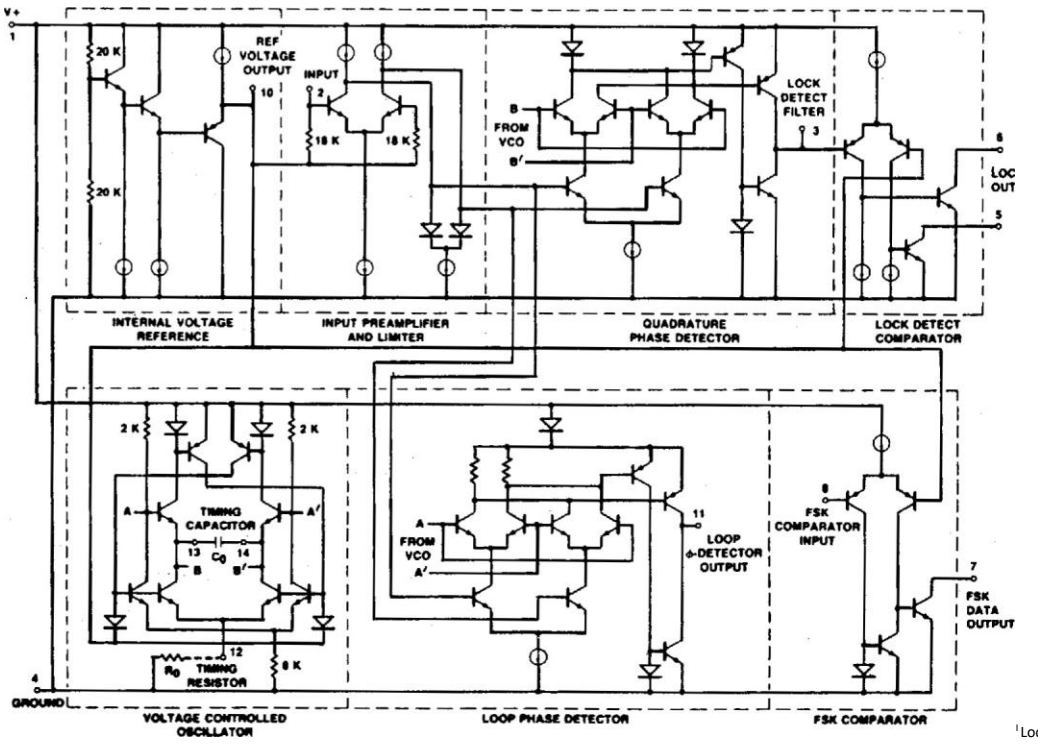
Figure 12. Linear FM Detector Using XR-2211 and an External Op Amp. (See Section an Design Equation for Component Values.)

The FM detector gain, i.e., the output voltage change

VOUT = RI VR/IOO Ro Volts/% deviation

where VR is the internal reference voltage (VR = V + /2 — 650mV). For the choice of external components RI, Roj CD, Cl and CF, see section on design equations.

EQUIVALENT SCHEMATIC DIAGRAM



^{I}Locx
OUTPUTSDETECT